10.2: Measuring Key Transport Properties of FET Devices

Field Effect Transistors

Arguably the most important invention of modern times, the transistor was invented in 1947 at Bell Labs by John Bardeen, William Shockley, and Walter Brattain. The result of efforts to replace inefficient and bulky vacuum tubes in current regulation and switching functions. Further advances in transistor technology led to the field effect transistors (FETs), the bedrock of modern electronics. FETs operate by utilizing an electric field to control the flow of charge carriers along a channel, analogous to a water valve to control the flow of water in your kitchen sink. The FET consists of 3 terminals, a source (S), drain (D), and gate (G). The region between the source and drain is called the channel. The conduction in the channel depends on the availability of charge carriers controlled by the gate voltage. Figure depicts a typical schematic and Figure 10.2.1 the associated cross-section of a FET with the source, draing and gate terminals labeled. FETs come in a variety of flavors depending on their channel doping (leading to enhancement and depletion modes) and gate types, as seen in Figure 10.2.2 The two FET types are junction field effect transistors (JFETs) and metal oxide semiconductor field effect transistors (MOSFETs).

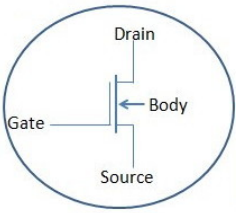

Figure 10.2.1 The n-channel enhancement mode MOSFET symbol.

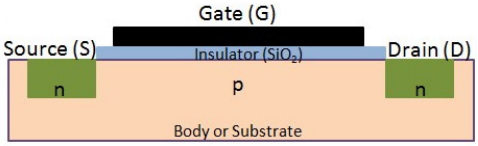

Figure 10.2.2 A typical cross-section of a n-channel enhancement mode MOSFET.

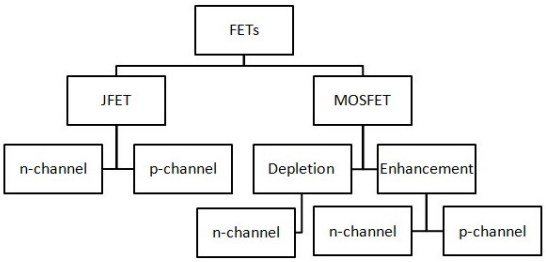

Figure 10.2.3 Field effect transistor family tree. Adapted from P. Horowitz and W. Hill, in *Art of Electronics*, Cambridge University Press, New York, 2nd Edn., 1994.

JFET Fundamentals

Junction field effect transistors (JFETs) as their name implies utilize a PN-junction to control the flow of charge carriers. The PN-junction is formed when opposing doping schemes are broght together on both sides of the channel. The doping schemes can be made to be either n-type (electrons) or p-type (holes) by doping with boron/gallium or phosphorus/arsenic respectively. The n-channel JFETs consists of pnp junctions where the source and drain are n-doped and the gate is p-doped. Figure 10.2.4 shows the cross section of a n-channel JFET in the “ON” state obtained by applying a positive drain-source voltage in the absence of a gate-source voltage. Alternatively the p-channel JFET consists of npn junctions where the source and drain are p-doped and the gate is n-doped. For p-channel a negative drain-source voltage is applied in the absence of a gate voltage to turn “ON” the npn device, as seen in Figure 10.2.5. Since JFETs are “ON” when no gate-source voltage is applied they are called depletion mode devices. Meaning that a depletion region is required to turn “OFF” the device. This is where the PN-junction comes into play. The PN-junction works by enabling a depletion region to form where electrons and holes combine leaving behind positive and negative ions which inhibit further charge transfer as well as depleting the availability of charge carriers at the interface. This depletion region is pushed further into the channel by applying a gate-source voltage. If the voltage is sufficient the depletion region on either side of the channel will “pinch off” the flow through the channel and the device will be “OFF”. This voltage is called the pinch off voltage,

V_P. The n-channel V_P is obtained by increasing the gate-source voltage in the negative direction, while the p-channel V_P is obtained by increasing the gate-source voltage in the positive direction.

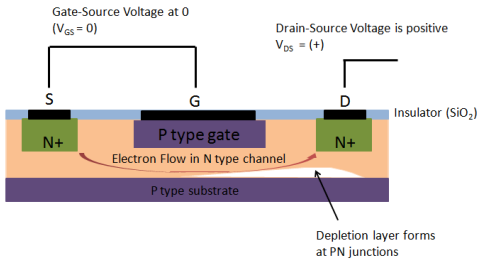

Figure 10.2.4 Cross-section of a n-channel JFET in the "ON" state.

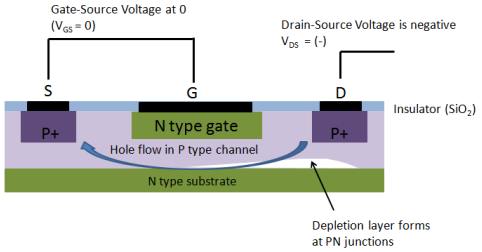

Figure 10.2.5 Cross-section of a p-channel JFET in the "ON" state.

MOSFET Fundamentals

The metal oxide semiconductor field effect transistor (MOSFET) utilizes an oxide layer (typically SiO2) to isolate the gate from the source and drain. The thin layer of oxide prevents flow of current to the gate, but enables an electric field to be applied to the channel which regulates the flow of charge carriers through the channel.MOSFETs unlike JFETs can operate in depletion or enhancement mode characterized by their ON or OFF state at zero gate-source voltage, VGS.

For depletion mode MOSFETs the device is “ON” when the VGS is zero as a result of the devices structure and doping scheme. The n-channel depletion mode MOSFET consists of heavily n-doped source and drain terminals on top of a p-doped substrate. Underneath an insulating oxide layer there is a thin layer of n-type silicon which allows charge carriers to flow in the absence of a gate voltage. When a negative voltage is applied to the gate a depletion region forms inside the channel, as seen in Figure. If the gate voltage is sufficient the depletion region pinches off the flow of electrons.

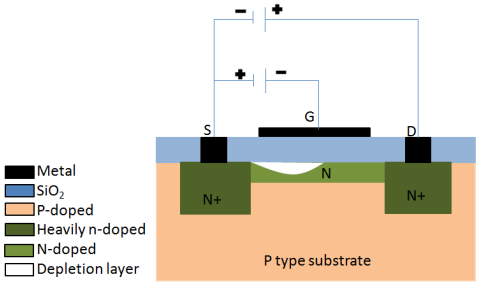

Figure 10.2.6 Cross-section of a n-channel depletion mode MOSFET when a negative gate voltage is applied with the resultant depletion layer.

For enhancement mode MOSFETs the ON state is attained by applying a gate voltage in the direction of the drain voltage; a positive voltage for n-channel enhancement MOSFETs, and a negative voltage for p-channel enhancement MOSFETs. The term “enhancement” is derived from the increase in conductivity seen by applying a gate voltage. This increase in conductivity is enabled by an inversion layer induced by the applied electric field at the gate as shown in Figure 10.2.7for n-channel enhancement mode MOSFETs and Figure 10.2.8for p-channel enhancement mode MOSFETs respectively.

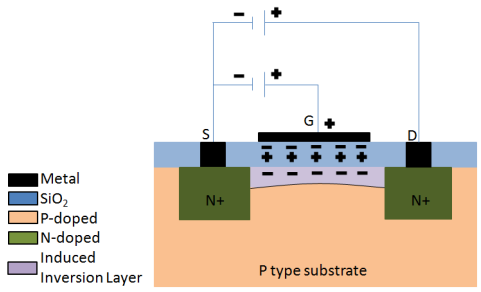

Figure 10.2.7 A depiction of the induced inversion layer with n-type charge carriers in a n-channel enhancement mode MOSFET.

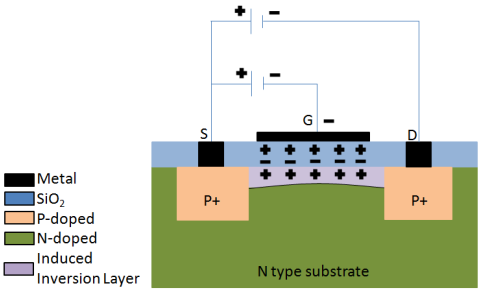

Figure 10.2.8 A depiction of the induced inversion layer with p-type charge carriers in a p-channel enhancement mode MOSFET.

The thickness of this inversion layer is controlled by the magnitude of the gate voltage. The minimum voltage required to form the inversion layer is called the gate-to-source threshold voltage, V_T. In the case of n-channel enhancement mode MOSFETs, the "ON" state is reached when $V_{GS} > V_T$ and a positive drain-source voltage, V_{DS}, is applied. If the V_{GS} is too low, then increasing the V_{DS} further results only in increasing the depletion region around the drain. The p-channel enhancement mode MOSFETs operate similarly except that the voltages are reversed. Specifically, the "ON" state occurs when $V_{GS} < V_T$ and a negative drain-source voltage is applied.

Measurement of key FET Parameters

In both an academic and industrial setting characterization of FETs is beneficial for determining device performance. Identifying the quality and type of FET can easily be addressed by measuring the transport characteristics under different experimental conditions utilizing a semiconductor characterization system (SCS). By analyzing the V-I characteristics through what are called voltage sweeps, the following key device parameters can be determined:

Pinch off Voltage V_p

The voltage needed to turn "OFF" a JFET. When designing circuits it is essential that the pinch-off voltage be determined to avoid current leakage which can dramatically reduce performance.

Threshold Voltage V_T

The voltage needed to turn "ON" a MOSFET. This is a critical parameter in effective circuit design.

Channel Resistance R_{DS}

The resistance between the drain and source in the channel. This influences the amount of current being transferred between the two terminals.

Power Dissipation P_D

The power dissipation determines the amount of heat generated by the transistor. This becomes a real problem since the transport properties deteriorate as the channel is heated.

Effective Charge Carrier Mobility μ_n

The charge carrier mobility determines how quickly the charge carrier can move through the channel. In most cases higher mobility leads to better device performance. The mobility can also be used to gauge the impurity, defect, temperature, and charge carrier concentrations.

Transconductance gain g_m (transfer admittance)

The gm is a measure of gain or amplification of a current for a given change in gate voltage. This is critical for amplification type electronics.

Equipment Needs

PC with Keithley Interactive Test Environment (KITE) software.

Semiconductor characterization system (Keithley 4200-SCS or equivalent).

Probe station.

Probe tips.

Protective gloves.

Measurement (V-I) Characteristics

The Semiconductor Characterization System is an automated system that provides both (V-I) and (V-C) characterization of semiconductor devices and test structures. The advanced digital sweep parameter analyzer provides sub-micron characterization with accuracy and speed. This system utilizes the Keithley Interactive Test Environment (KITE) software designed specifically for semiconductor characterization.

Procedure

1. Connect the probe tips to the probe station. Then attach the banana plugs from the probe station to the BNC connector, making sure not to connect to ground.
2. Select the appropriate connections for your test from Table 10.2.1
3. Place your transistor sample on the probe station, but don't let the probe tips touch the sample to prevent possible electric shock(during power up, the SMU may momentarily output high voltage).
4. Turn on power located on the lower right of the front panel. The power up sequence may take up to 2 minutes.
5. Start KITE software. Figure 10.2.9shows the interface window.
6. Select the appropriate setup from the Project Tree drop down (top left).
7. Match the Definition tab terminal connections to the physical connections of probe tips. If connection is not yet matched you can assign/reassign the terminal connections by using the arrow key next to the instrument selection box that displays a list of possible connections. Select the connection in the instrument selection box that matches the physical connection of the device terminal.
8. Set the Force Measure settings for each terminal. Fill in the necessary function parameters such as start, stop, step size, range, and compliance. For typical voltage sweeps you'll want to force the voltage between the drain and source while measuring the current at the drain. Make sure to conduct several voltage sweeps at various forced gate voltages to aid in the analysis.
9. Check the current box/voltage box if you desire the current/voltage to be recorded in the Sheet tab Data worksheet and be available for plotting in the Graph tab.
10. Now make contact to your sample with the probe tips
11. Run the measurement setup by clicking the green Run arrow on the tool bar located above the Definition tab. Make sure the measuring indicator light at bottom right hand corner of the front panel is lit.
12. Save data by clicking on the Sheet tab then selecting the Save As tab. Select the file format and location.

Table 10.2.1 Connection selection.

Connection	Description
SMU1	Medium power with low noise preamplifier
SMU2	Medium power source without preamplifier
SMU3	High Power
GNRD	For large currents

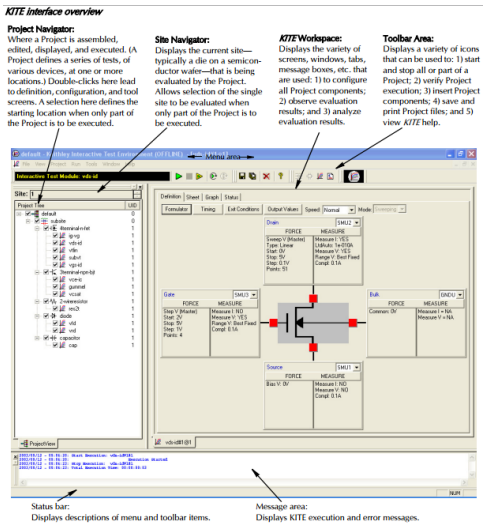

Figure 10.2.9 Keithley Interactive Test Environment (KITE) interface window.

Measurement Analysis

Typical V-I Characteristics of JFETs

Voltage sweeps are a great way to learn about the device. Figure 10.2.10 shows a typical plot of drain-source voltage sweeps at various gate-source voltages while measuring the drain current, ID for a n-channel JFET. The V-I characteristics have four distinct regions. Analysis of these regions can provides critical information about the device characteristics such as the pinch off voltage, VP, transcunductance gain, gm, drain-source channel resistance, RDS, and power dissipation, PD.

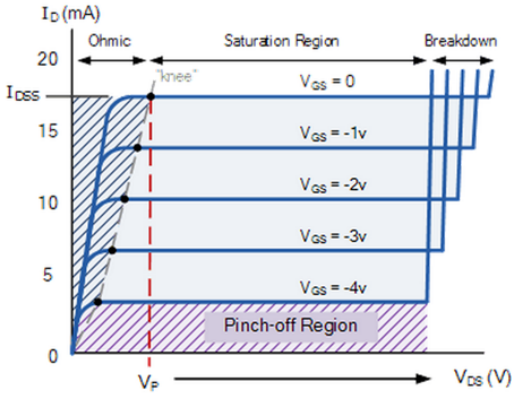

Figure adapted from Electronic Tutorials (www.electronic-tutorials.ws).

Ohmic Region (Linear Region)

This region is bounded by VDS < VP. Here the JFET begins to flow a drain current with a linear response to the voltage, behaving like a variable resistor. In this region the drain-source channel resistance, RDS is modeled by 10.2.1, where ΔVDS is the change in drain-source voltage, ΔID is the change in drain current, and gm is the transcunductance gain. Solving for gm results in 10.2.2.

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m} \tag{10.2.1}$$

$$g_m = \frac{\Delta I_D}{\Delta V_{DS}} = \frac{1}{R_{DS}} \tag{10.2.2}$$

Saturation Region

This is the region where the JFET is completely “ON”. The maximum amount of current is flowing for the given gate-source voltage. In this region the drain current can be modeled by the 10.2.3, where ID is the drain current, IDSS is the maximum current, VGS is the gate-source voltage, and VP is the pinch off voltage. Solving for the pinch off voltage results in 10.2.4.

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P}) \tag{10.2.3}$$

$$V_P = 1 - \frac{V_{GS}}{\sqrt{\frac{I_D}{I_{DSS}}}} \tag{10.2.4}$$

Breakdown Region

This region is characterized by the sudden increase in current. The drain-source voltage supplied exceeds the resistive limit of the semiconducting channel, resulting in the transistor to break down and flow an uncontrolled current.

Pinch-off Region (Cutoff Region)

In this region the gate-source voltage is sufficient to restrict the flow through the channel, in effect cutting off the drain current. The power dissipation, PD, can be solved utilizing Ohms law (I = V/R) for any region using 10.2.5.

$$P_D = I_D \times V_{DC} = (I_D)^2 \times R_{DS} = (V_{DS})^2 / R_{DS} \tag{10.2.5}$$

The p-channel JFET V-I characteristics behave similarly except that the voltages are reversed. Specifically, the pinch off point is reached when the gate-source voltage is increased in a positive direction, and the saturation region is met when the drain-source voltage is increased in the negative direction.

Typical V-I Characteristics of MOSFETs

Figure 10.2.11 shows a typical plot of drain-source voltage sweeps at various gate-source voltages while measuring the drain current, I_D for an ideal n-channel enhancement MOSFET. Like JFETs, the V-I characteristics of MOSFETS have distinct regions that provide valuable information about device transport properties.

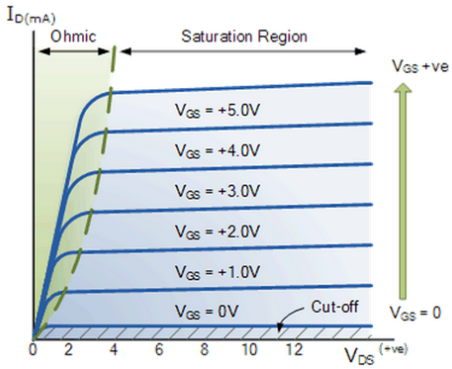

Figure adapted from Electronic Tutorials (www.electronic-tutorials.ws).

Ohmic Region (Linear Region)

The n-channel enhanced MOSFET behaves linearly, acting like a variable resistor, when the gate-source voltage is greater than the threshold voltage and the drain-source voltage is greater than the gate-source voltage. In this region the drain current can be modeled by 10.2.6, where ID is the drain current, VGS is the gate-source voltage, VT is the threshold voltage, VDS is the drain-source voltage, and k is the geometric factor described by 10.2.7, where μ_n is the charge-carrier effective mobility, C_{OX} is the gate oxide capacitance, W is the channel width, and L is the channel length.

$$I_D = 2k(V_{GS} - V_T)V_{DS} - [(V_{DS})^2/2] \tag{10.2.6}$$

$$k = \mu_n C_{OX} \frac{W}{L} \tag{10.2.7}$$

Saturation Region

In this region the MOSFET is considered fully “ON”. The drain current for the saturation region is modeled by 10.2.8. The drain current is mainly influenced by the gate-source voltage, while the drain-source voltage has no effect.

$$I_D = k(V_{GS} - V_T)^2 \tag{10.2.8}$$

Solving for the threshold voltage VT results in 10.2.9.

$$V_T = V_{GS} - \sqrt{\frac{I_D}{k}} \tag{10.2.9}$$

Pinch-off Region (Cutoff Region)

When the gate-source voltage, VGS, is below the threshold voltage VT the charge carriers in the channel are not available “cutting off” the charge flow. Power dissipation for MOSFETs can also be solved using equation 6 in any region as in the JFET case.

FET V-I Summary

The typical I-V characteristics for the whole family of FETs seen in Figure 10.2.11are plotted in Figure 10.2.12

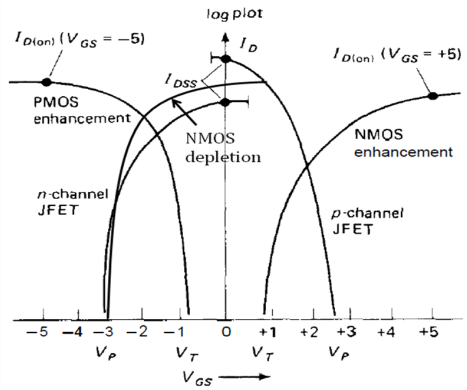

Figure 10.2.12 Plot of V-I characteristics for the various FET types. Adapted from P. Horowitz and W. Hill, in *Art of Electronics*, Cambridge University Press, New York, 2nd Edn., 1994.

From Figure 10.2.12we can see how the doping schemes that lead to enhancement and depletion are displaced along the VGS axis. In addition, from the plot the ON or OFF state can be determined for a given gate-source voltage, where (+) is positive, (0) is zero, and (-) is negative, as seen in Table 10.2.1.

Table 10.2.1: The ON/OFF state for the various FETs at a given gate-source voltages where (-) is a negative voltage and (+) is a positive voltage.

FET Type	V_{GS} = (-)	V_{GS} = 0	V_{GS} = (+)
n-channel JFET	OFF	ON	ON
p-channel JFET	ON	ON	OFF
n-channel depletion MOSFET	OFF	ON	ON
p-channel depletion MOSFET	ON	ON	OFF
n-channel enhancement MOSFET	OFF	OFF	ON
p-channel enhancement MOSFET	ON	ON	OFF