LABORATORY MANUAL: OPERATIONAL AMPLIFIERS AND LINEAR INTEGRATED CIRCUITS

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Licensing

A detailed breakdown of this resource's licensing can be found in ***Back Matter/Detailed Licensing***.

CHAPTER OVERVIEW

1: Decibels and Bode Plots

Objective

In this exercise, the usage of decibel measurements and Bode plots will be examined. The investigation will include the relationship between ordinary and decibel gain, and the decibel-amplitude and phase response of a simple lag network.

1.1: Theory Overview

The decibel is a logarithmic-based measurement scheme. It is based on ratios of change. Positive values indicate an increase while negative values indicate a decrease. Decibel schemes can be used for gains and, with minor modification, signal levels. A Bode plot shows the variations of gain (typically expressed in decibels) and phase across a range of frequencies for some particular circuit. These will prove to be very valuable in later design and analysis work.

1.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 1.2, The Decibel

Section 1.3, Bode Plots

1.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) Decibel-reading voltmeter

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

1.4: Components

(1) 100n F

actual:___________________

(1) 100 Ω

actual:___________________

(1) 1k Ω

actual:___________________

(1) 4k7 Ω

actual:___________________

(2) 10k Ω

actual:___________________ ___________________

(1) 22k Ω

actual:___________________

1.5: Schematics

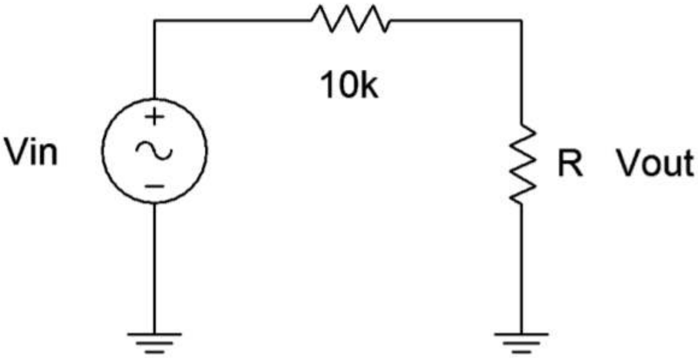

Figure 1.5.1

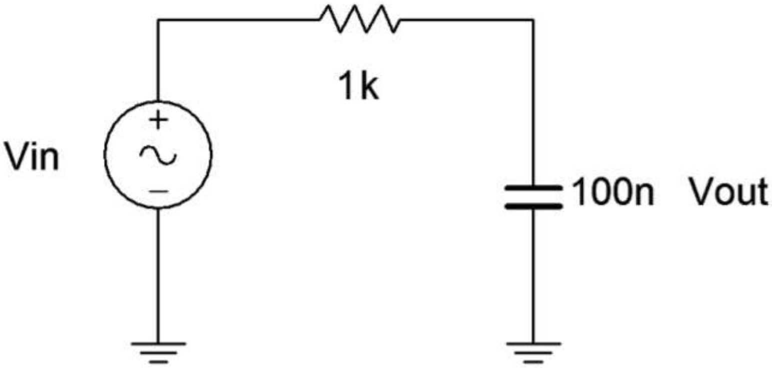

Figure 1.5.2

1.6: Procedure

1. Calculate the voltage gains (losses) for the voltage divider of Figure 1.5.1 for the resistor values specified, and record them in Table 1.7.1. Also, convert each of the ordinary gains into decibel form.

2. Assemble the circuit of Figure 1.5.1 using the 22k resistor.

3. Set the generator to a 100 Hz sine wave, 0 dBV (Note: If the meter is calibrated in dBu, then use 0 dBu).

4. Apply the generator to the circuit. Measure and record the output voltage in Table 1.7.1 using the decibel-reading voltmeter. Also, compute the resulting experimental decibel voltage gain and gain deviation.

5. Repeat step 4 for the remaining resistor values in Table 1.7.1.

6. To create a simple Bode plot, the lag network of Figure 1.5.2 will be used. Assemble this circuit and record its theoretical critical frequency in Table 1.7.2.

7. Set the generator to a 1 kHz sine wave, 0 dBV.

8. Apply the generator to the circuit. Determine the experimental critical frequency by adjusting the frequency of the generator until the circuit's output voltage is –3 dBV. Record the measured frequency in Table 1.7.2.

9. Set the generator to a sine wave at one-tenth of the experimental critical frequency.

10. Adjust the generator's output level to 0 dBV.

11. Apply the generator to the circuit. Measure and record the output level in decibels in Table 1.7.3. Also, measure and record the phase angle between the input and output waveforms and record it in Table 1.7.3.

12. Repeat steps 9 through 11 for the remaining frequencies listed in Table 1.7.3.

13. Using the values from Table 1.7.3, create a Bode plot for this circuit using a log scaled horizontal axis (i.e., semi-log paper).

1.6.1: Computer Simulation

14. Build the lag network of Figure 1.5.2 in a simulator and run an AC Analysis. Be sure to run this from at least one decade below the critical frequency to at least one decade above. Also, use a decibel scale for the gain amplitude. Compare the results to the Bode plot generated in Step 13 and include this graph with the technical report.

1.7: Data Tables

R	A_v Theory	A_v' Theory	V_{out}'	Experimental A_v'	% Deviation
22k Ω					
10k Ω					
4k7 Ω					
1k Ω					
100 Ω					

Table 1.7.1

Theoretical f_c	
Experimental f_c	

Table 1.7.2

Factor	Frequency	A_v'	Phase
.1 f_c			
.2 f_c			
.5 f_c			
f_c			
2 f_c			
5 f_c			
10 f_c			

Table 1.7.3

1.8: Questions

1. Is the logarithmic nature of the decibel apparent in the data of Table 1.7.1?

2. Using the plot created in step 13, determine the slope in dB-per-octave in the region above f_c.

3. What would the plot of step 13 look like if ordinary gains had been used instead of decibel gains?

CHAPTER OVERVIEW

2: The Differential Amplifier

Objective

In this exercise, the performance of a differential amplifier will be examined. The investigation will include the DC parameters of input bias and offset current, and output offset voltage. The AC parameters of interest are the differential and common-mode gains, and the resulting common-mode rejection-ratio (CMRR).

2.1: Theory Overview

The ideal differential amplifier is perfectly symmetrical producing identical DC input bias currents and output collector voltages. Several factors ranging from the mismatch of transistor parameters to resistor tolerances prevent perfect symmetry in a practical circuit. The DC quality of the circuit can be expressed in terms of the mismatches. The difference between the input bias currents is known as the input offset current. The difference between the output collector voltages is known as the output offset voltage. For AC performance, the primary items of concern are the differential and common-mode gains. The ideal differential amplifier will only amplify differential input signals, and thus, has a common-mode gain of zero. Due to component mismatches and internal design limits, the common-mode gain is never zero, allowing some portion of the common-mode input signal to make its way to the output. The measure of the suppression of common-mode signals is given by the common-mode rejection-ratio, or CMRR. CMRR can be found by dividing the differential gain by the common-mode gain.

2.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 1.6, The Differential Amplifier

2.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

2.4: Components

(3) Small signal NPN transistors (2N3904, 2N2222, etc.)

(2) 100 Ω

actual:___________________ ___________________

(2) 330 Ω

actual:___________________ ___________________

(2) 470 Ω

actual:___________________ ___________________

(1) 3k3 Ω

actual:___________________

(2) 4k7 Ω

actual:___________________ ___________________

(1) 5k6 Ω

actual:___________________

(1) 10k Ω

actual:___________________

(2) 22k Ω

actual:___________________ ___________________

(1) 33k Ω

actual:___________________

2N3904 Datasheet: https://www.onsemi.com/pub/Collateral/2N3903-D.PDF

2.5: Schematics

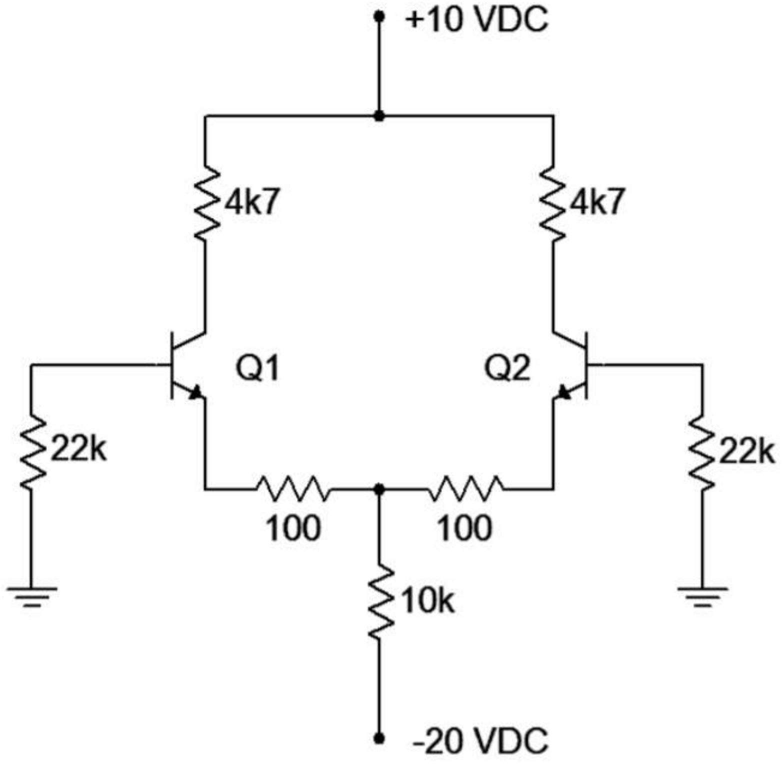

Figure 2.5.1

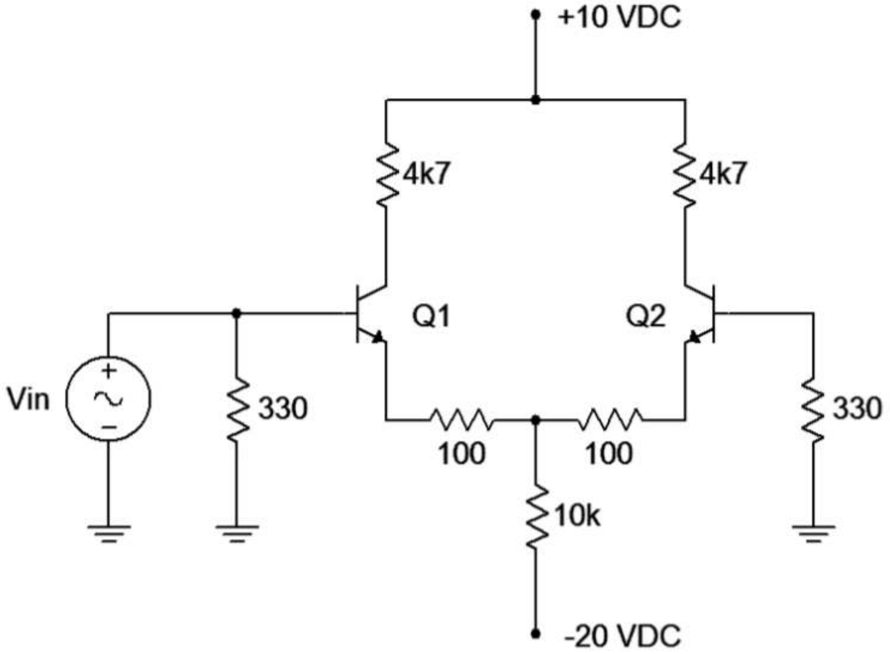

Figure 2.5.2

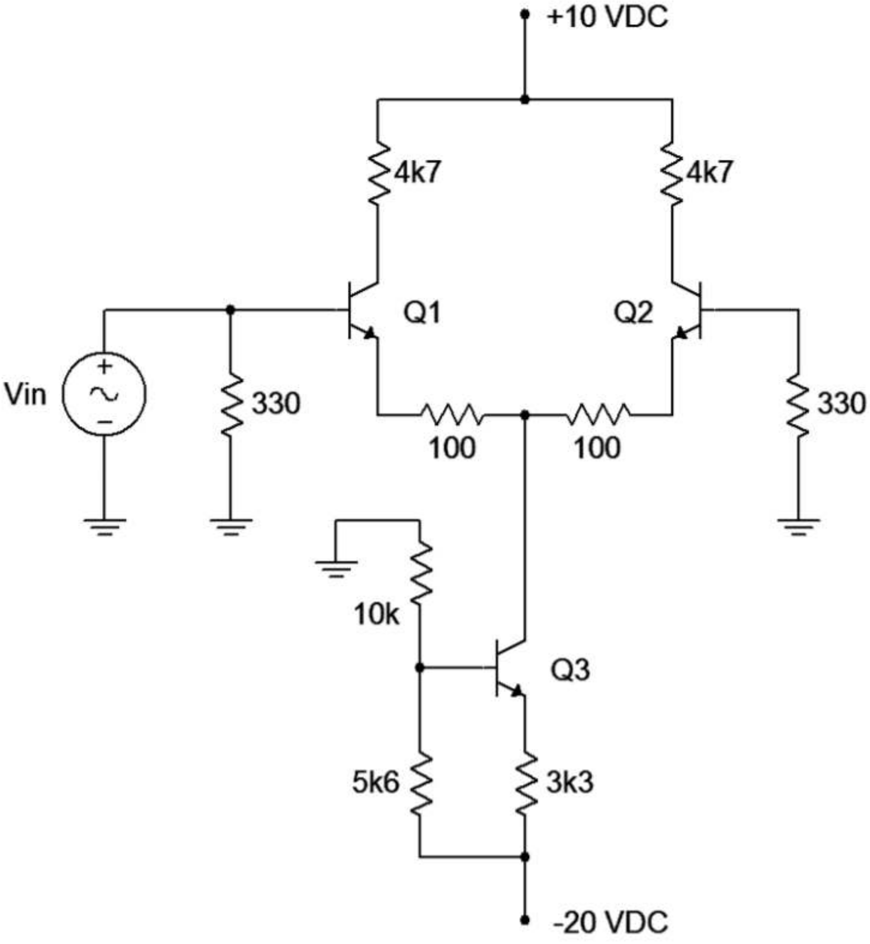

Figure 2.5.3

2.6: Procedure

2.6.1: DC Parameters

1. Assume that the transistors of Figure 2.5.1 have a current gain of 150. Calculate the base currents and collector voltages for the amplifier of Figure 2.5.1 and record them in Table 2.7.1. Also, compute and record the theoretical (ideal) input offset current and output offset voltage.

2. Assemble the circuit of Figure 2.5.1.

3. Measure and record the base currents in Table 2.7.1. (Note: You may wish to measure the voltage across the base resistors and compute the base currents if the DMM cannot measure small DC currents.) Based on these currents, compute and record the experimental input bias and offset currents along with the corresponding deviations.

4. Measure and record the collector voltages in Table 2.7.1. Based on these voltages, compute and record the experimental output offset voltage and the corresponding deviation.

2.6.2: AC Parameters

5. Calculate the differential voltage gain and collector voltages for the amplifier of Figure 2.5.2 using an input of 20 millivolts, and record them in Table 2.7.2.

6. Assemble the circuit of Figure 2.5.2.

7. Set the generator to a 1 kHz sine wave, 20 millivolts peak.

8. Apply the generator to the amplifier. Measure and record the AC collector voltages in Table 2.7.2 while noting the phase relative to the input. Also, compute the resulting experimental voltage gain from the input to collector one, and the deviations.

9. Apply the generator to both inputs. Set the generator’s output to 1 volt peak.

10. Measure the AC voltage at collector one and record it in Table 2.7.3.

11. Based on the value measured in step 10, compute and record the common-mode gain and CMRR in Table 2.7.3.

2.6.3: Improved CMRR

12. Assemble the circuit of Figure 2.5.3. This circuit uses an improved tail current source that exhibits much higher internal impedance than the circuit of Figure 2.5.2. This should yield a decrease in common mode gain which, in turn, should yield an improved CMRR. Note that the new circuit sets up virtually the same tail current, therefore producing approximately the same DC parameters and differential gain as the original.

13. Repeat steps 9 through 11 recording the results in Table 2.7.4.

2.6.4: Troubleshooting

14. Continuing with the amplifier of Figure 2.5.3, turn the signal down to 0. Estimate and then measure the results for each individual error presented in Table 2.7.5.

2.6.5: Computer Simulation

15. Build the amplifier of Figure 2.5.2 in a simulator and run a Transient Analysis echoing steps 5 through 8. Compare the results to the data found in Table 2.7.2.

2.7: Data Tables

DC Quantity	Theoretical	Experimental	% Deviation
I_{B1}			
I_{B2}			
$I_{in-bias}$			
$I_{in-offset}$			n/a
V_{C1}			
V_{C2}			
$V_{out-offset}$			n/a

Table 2.7.1

AC Quantity	Theoretical	Experimental	% Deviation
V_{C1}			
V_{C2}			
A_v			

Table 2.7.2

V_{C1}	
A_{cm}	
CMRR	

Table 2.7.3

V_{C1}	
A_{cm}	
CMRR	

Table 2.7.4

Error	Quantity	Estimate	Actual
3k3 is replaced with 33k	V_{C1} DC		
Q_1's 4k7 is 470	V_{C1} DC		
Both 4k7 are 470	V_{C1} DC		

Table 2.7.5

2.8: Questions

1. How might the input offset current of Figure 2.5.1 be reduced?

2. What are some causes of output offset voltage in the circuit of Figure 2.5.1?

3. What are the effects if the two collector resistors not identical in value?

4. What is the significance of a high CMRR?

5. How significant is the change in CMRR when using the improved current source? Based on the improvement, estimate the internal impedance of the current source.

CHAPTER OVERVIEW

3: The Op Amp Comparator

Objective

In this exercise, the performance of a typical op amp will be examined in the open-loop mode. This circuit is often referred to as a comparator. The investigation will include the effect of both DC and AC input signals.

3.1: Theory Overview

The open-loop voltage gain of the typical op amp is very high, approaching 100,000 at low frequencies. With such a high gain, even minute differences between the inverting and non-inverting input signals will be magnified to the point of causing saturation. Thus, if the non-inverting input signal exceeds the inverting input signal, the output will be at positive saturation. If the signals are reversed, then negative saturation results. If both inputs are identical, then the output will go to either positive or negative saturation, depending on the internal offsets of the op amp.

3.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 2.2, What Is An Op Amp?

3.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

3.4: Components

(1) General purpose op amp (741, 351, 411, 081, etc.)

(2) 1μ F actual:__________________ __________________

(1) 2k2 Ω actual:__________________

(1) 4k7 Ω actual:__________________

(2) 10k Ω actual:__________________ __________________

(1) 15k Ω actual:__________________

(1) 22k Ω actual:__________________

LM741 Datasheet: http://www.ti.com/lit/ds/symlink/lm741.pdf

LF351 Datasheet: https://www.st.com/resource/en/datasheet/lf351.pdf

LF411 Datasheet: http://www.ti.com/lit/ds/symlink/lf411.pdf

TL081 Datasheet: http://www.ti.com/lit/ds/symlink/tl081.pdf

3.5: Schematics

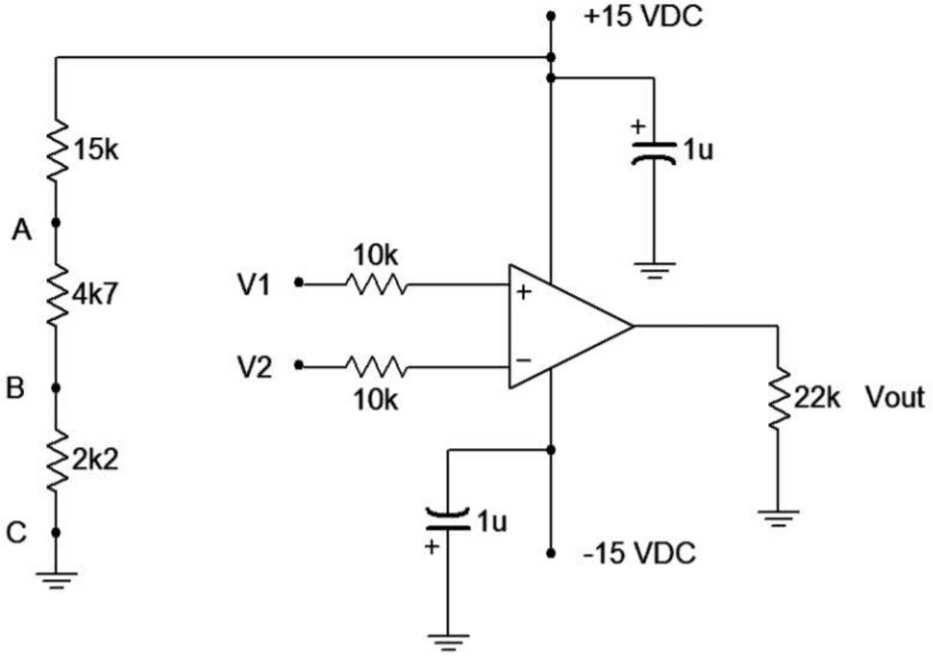

Figure 3.5.1

3.6: Procedure

1. Calculate the voltages at points A, B, and C, and record them in Table 3.7.1.

2. Assemble the circuit of Figure 3.5.1.

3. Using the input combinations listed in Table 3.7.2, apply the appropriate signals to V_1 and V_2. Measure the output signal using the oscilloscope, and record the values in Table 3.7.2.

4. Connect V_1 to a 10 volt peak-to-peak 1 kHz sine wave. Make sure the oscilloscope inputs are set to DC Coupling, and then connect probe 1 to V_1, probe 2 to V_2 and probe 3 to V_{out}.

5. Connect V_2 to point A. Measure the output voltage and save a copy of the oscilloscope display as Graph 1.

6. Connect V_2 to point B. Measure the output voltage and save a copy of the oscilloscope display as Graph 2.

7. Connect V_2 to point C. Measure the output voltage and save a copy of the oscilloscope display as Graph 3.

3.6.1: Computer Simulation

8. Build the circuit of Figure 3.5.1 in a simulator and run a Transient Analysis echoing steps 4 through 7. Compare the results to the waveforms generated experimentally.

3.7: Data Tables

Connection Node	Voltage
A	
B	
C	

Table $3.7.1$

V_1	V_2	V_{out}
A	A	
A	B	
A	C	
B	A	
B	B	
B	C	
C	A	
C	B	
C	C	

Table $3.7.2$

3.8: Questions

1. What happens when $V_1 > V_2$? Why?

2. What happens when $V_1 < V_2$? Why?

3. What happens when $V_1 = V_2$? Why?

4. Explain the differences in the waveforms recorded in Graphs 1 through 3.

5. How would the waveform displays be altered if the oscilloscope inputs were set to AC Coupling instead of DC Coupling in step 4?

6. How would the results of this exercise change if the op amp had a very low gain, say only 1 or 2?

CHAPTER OVERVIEW

4: The Non-inverting Voltage Amplifier

Objective

In this exercise, the performance of the non-inverting voltage amplifier will be examined. The investigation will include the effect of feedback resistors on setting voltage gain, stability of gain with differing op amps, and input impedance.

4.1: Theory Overview

The non-inverting voltage amplifier is based on series-parallel negative feedback. As the ideal voltage-controlled voltage source, this amplifier exhibits high input impedance, low output impedance, and stable voltage gain. The voltage gain is set by the two feedback resistors, R_i and R_f.

4.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 3.4, The Four Variants of Negative Feedback

Section 4.2, Inverting and Non-inverting Amplifiers

4.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

4.3.1: For Distortion Measurement Only

(1) Low distortion sine source

model:_________________ srn:___________________

(1) Distortion analyzer

model:_________________ srn:___________________

4.4: Components

(3) General purpose op amps (1 each of 741, 351, 318, 411, 081, etc.)

(2) 1μ F

actual:__________________ __________________

(1) 1k Ω

actual:__________________

(1) 4k7 Ω

actual:__________________

(1) 10k Ω

actual:__________________

(1) 22k Ω

actual:__________________

(1) 33k Ω

actual:__________________

(1) 47k Ω

actual:__________________

(1) 100k Ω

actual:__________________

LM741 Datasheet: http://www.ti.com/lit/ds/symlink/lm741.pdf

LF351 Datasheet: https://www.st.com/resource/en/datasheet/lf351.pdf

LF411 Datasheet: http://www.ti.com/lit/ds/symlink/lf411.pdf

LM318 Datasheet: http://www.ti.com/lit/ds/symlink/lm318-n.pdf

TL081 Datasheet: http://www.ti.com/lit/ds/symlink/tl081.pdf

4.5: Schematics

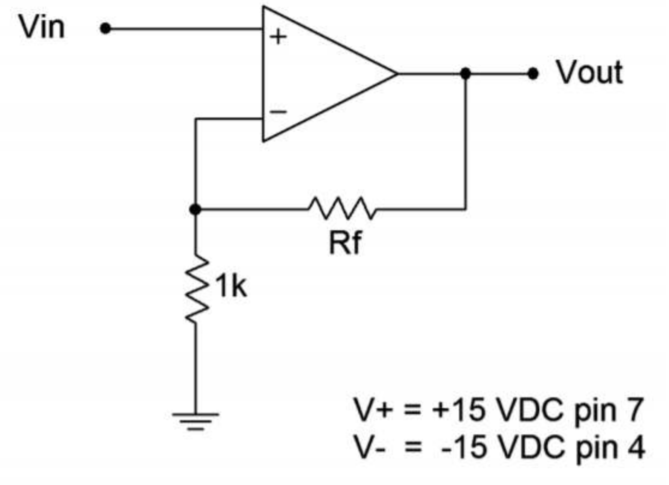

Figure 4.5.1

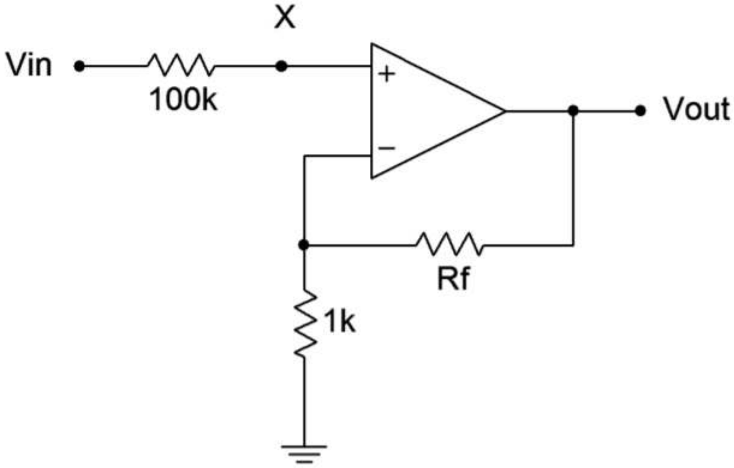

Figure 4.5.2

4.6: Procedure

1. The voltage gain of the non-inverting amplifier can be determined accurately from the feedback resistors R_i and R_f. Calculate the voltage gains for the amplifier of Figure 4.5.1 for the R_f values specified, and record them in Table 4.7.1.

2. Assemble the circuit of Figure 4.5.1 using the 4k7 Ω resistor.

3. Set the generator to a 1 kHz sine wave, 100 millivolts peak.

4. Apply the generator to the amplifier. Measure and record the output voltage in Table 4.7.1. Also, compute the resulting experimental voltage gain and gain deviation.

5. Repeat step 4 for the remaining R_f values in Table 4.7.1.

6. For any given R_i, R_f combination, the voltage gain should be stable regardless of the precise op amp used, even if it is of an entirely different model. To verify this, first set R_f to 22k Ω.

7. Set the generator to a 1 kHz sine wave, 100 millivolts peak.

8. Apply the generator to the amplifier. Measure and record the output voltage in Table 4.7.2. Also, compute the resulting experimental voltage gain and gain deviation.

9. Repeat step 8 for two other op amps.

10. It is not practical to use an ohmmeter to determine the input impedance of an active circuit. Instead, input impedance can be found by utilizing the voltage divider effect. Modify the circuit by adding the extra input resistor as shown in Figure 4.5.2.

11. Set R_f to 4k7 Ω.

12. Set the generator to a 200 Hz sine wave, 1 volt peak.

13. Apply the generator to the amplifier. Use a DMM to measure and record the AC potential from V_{in} to point X (i.e.,V_A, the voltage across the 100k) in Table 4.7.3. Using KVL, determine the voltage from point X to ground (V_B) and record in Table 4.7.3 (don’t forget to compensate for peak versus RMS readings). Finally, compute the resulting input impedance by using the voltage divider rule. Note: If the DMM is not sensitive enough and registers 0 volts for V_A, it is safe to assume that Z_{in} is considerably larger than the 100k Ω sensing resistor.

4.6.1: Distortion Measurement

14. Return to the amplifier of Figure 4.5.1 with R_f set to 10k Ω. If available, the LF351 is a good choice for the op amp in this portion. Replace the general purpose generator with the low distortion sine source set to 1 kHz. Adjust its output level so that the output of the op amp is approximately 0 dBV.

15. Apply the distortion analyzer to the output of the op amp, read the resulting THD percentage and record it in Table 4.7.4.

16. Repeat steps 14 and 15 using the remaining R_f values in Table 4.7.4.

4.6.2: Troubleshooting

17. Continuing with the amplifier of Figure 4.5.1, reset R_f to 4k7 Ω. Estimate and then measure the results for each individual error presented in Table 4.7.5.

4.7: Data Tables

R_f	Theoretical A_v	V_{out}	Experimental A_v	% Deviation
4k7 Ω				
10k Ω				
22k Ω				
33k Ω				
47k Ω				

Table 4.7.1

Op Amp	Theoretical A_v	V_{out}	Experimental A_v	% Deviation
1				
2				
3				

Table 4.7.2

V_A	V_B	Z_{in}

Table 4.7.3

R_f	% THD
10k Ω	
22k Ω	
47k Ω	

Table 4.7.4

Error	Quantity	Estimate	Actual
R_i's third band is orange	V_{out}		
f_{in} is 100 Hz	V_{out}		
R_i is swapped with R_f	V_{out}		
+ and – signal input pins swapped	V_{out}		

Table 4.7.5

4.8: Questions

1. What is the effect as R_f is increased?

2. How does the voltage gain vary as the op amp is changed?

3. Does the non-inverting voltage amplifier exhibit a predictable and stable voltage gain?

4. What can be said about the input impedance of this type of amplifier?

5. What is the relationship between gain, feedback and distortion?

CHAPTER OVERVIEW

5: The Inverting Voltage Amplifier

Objective

In this exercise, the performance of the inverting voltage amplifier will be examined. The investigation will include the effect of feedback resistors on setting voltage gain, stability of gain with differing op amps, and the concept of virtual ground.

5.1: Theory Overview

The inverting voltage amplifier is based on parallel-parallel negative feedback. This amplifier exhibits modest input impedance, low output impedance, and stable inverting voltage gain. The voltage gain is set by the two feedback resistors, R_i and R_f.

5.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 4.2, Inverting and Non-inverting Amplifiers

5.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

5.4: Components

(3) General purpose op amps (1 each of 741, 351, 318, 411, 081, etc.)

(2) 1μ F

actual:____________________ ____________________

(1) 1k Ω

actual:____________________

(1) 4k7 Ω

actual:____________________

(1) 10k Ω

actual:____________________

(1) 22k Ω

actual:____________________

(1) 33k Ω

actual:____________________

(1) 47k Ω

actual:____________________

5.5: Schematics

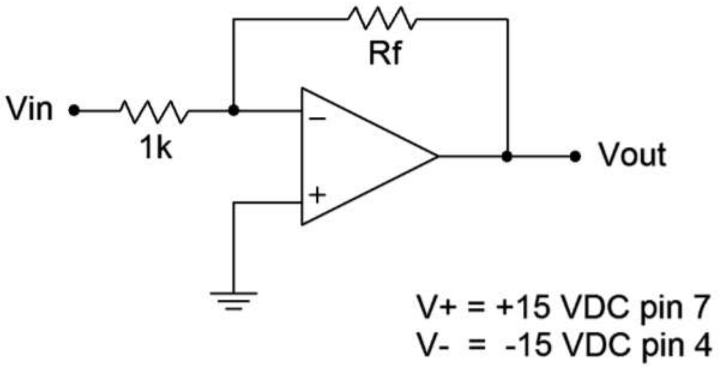

Figure 5.5.1

5.6: Procedure

1. The voltage gain of the inverting amplifier can be determined accurately from the feedback resistors R_i and R_f. Calculate the voltage gains for the amplifier of Figure 5.5.1 for the R_f values specified, and record them in Table 5.7.1.

2. Assemble the circuit of Figure 5.5.1 using the 4k7 Ω resistor.

3. Set the generator to a 1 kHz sine wave, 100 millivolts peak.

4. Apply the generator to the amplifier. Measure and record the output voltage in Table 5.7.1, noting its phase relative to the input. Also, compute the resulting experimental voltage gain and gain deviation.

5. Repeat step 4 for the remaining R_f values in Table 5.7.1.

6. For any given R_i, R_f combination, the voltage gain should be stable regardless of the precise op amp used, even if it is of an entirely different model. To verify this, first set R_f to 22k Ω.

7. Set the generator to a 1 kHz sine wave, 100 millivolts peak.

8. Apply the generator to the amplifier. Measure and record the output voltage in Table 5.7.2. Also, compute the resulting experimental voltage gain and gain deviation.

9. Repeat step 8 for two other op amps.

10. The concept of virtual ground is very important. A virtual ground exists at the inverting input of the op amp in this circuit. Ideally, the voltage at this point should be very close to 0. Through voltage divider effect, this implies that all of the input signal must be dropping across R_i, and thus R_i must establish the input impedance of the amplifier.

11. Set R_f to 4k7 Ω.

12. Set the generator to a 200 Hz sine wave, 1 volt peak.

13. Apply the generator to the amplifier. Use a DMM to measure and record the AC potential at the inverting terminal of the op amp. Record the value in Table 5.7.3.

5.6.1: Computer Simulation

14. Build the circuit in a simulator and run a Transient Analysis echoing steps 2 through 5. Compare the results to the waveforms generated experimentally.

15. Repeat step 14 but this time use the Distortion Analyzer instrument to compare voltage gain to THD.

5.7: Data Tables

R_f	A_v Theory	V_{out}'	Phase	Experimental A_v	% Deviation
4k7 Ω					
10k Ω					
22k Ω					
33k Ω					
47k Ω					

Table 5.7.1

Op Amp	A_v Theory	V_{out}	Experimental A_v	% Deviation
1				
2				
3				

Table 5.7.2

V_{inverting-input}\)	

Table 5.7.3

5.8: Questions

1. What is the effect as R_f is increased?
2. How does the voltage gain vary as the op amp is changed?
3. Does the inverting voltage amplifier exhibit a predictable and stable voltage gain?
4. What can be said about the input impedance of this type of amplifier?
5. Based on the simulation, what is the relationship between gain, feedback and distortion for this circuit?

CHAPTER OVERVIEW

6: The Op Amp Differential Amplifier

Objective

In this exercise, the performance of an op amp based differential amplifier will be examined. The investigation will include the effects of differential gain and common-mode rejection ratio (CMRR).

6.1: Theory Overview

An op amp differential amplifier can be created by combining both a non-inverting voltage amplifier and an inverting voltage amplifier in a single stage. Proper gain matching between the two paths is essential to maximize the common-mode rejection ratio. Differential gain is equal to the gain of the inverting path.

6.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 4.2, Inverting and Non-inverting Amplifiers

6.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

6.4: Components

(2) General purpose op amps (741, 351, etc.)

(2) 1 μF

actual:___________________ ___________________

(2) 10 kΩ

actual:___________________ ___________________

(1) 15 kΩ

actual:___________________

(1) 22 kΩ

actual:___________________

(2) 100 kΩ

actual:___________________ ___________________

(1) 10 kΩ potentiometer

6.5: Schematics

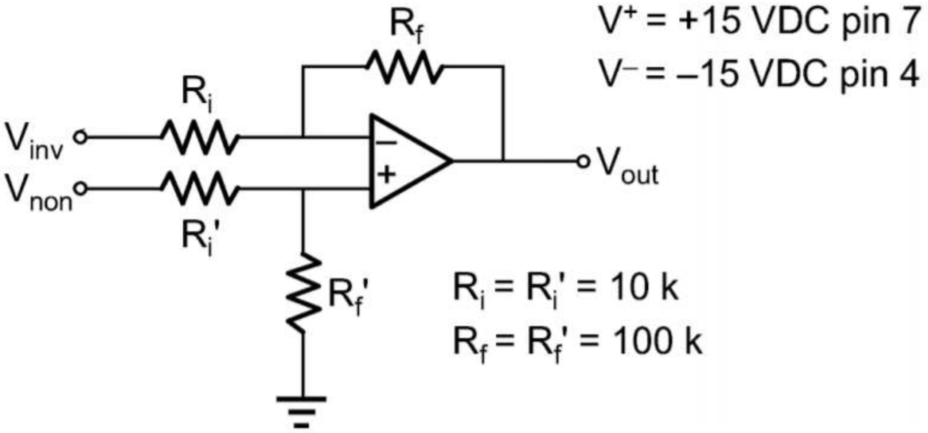

Figure 6.5.1

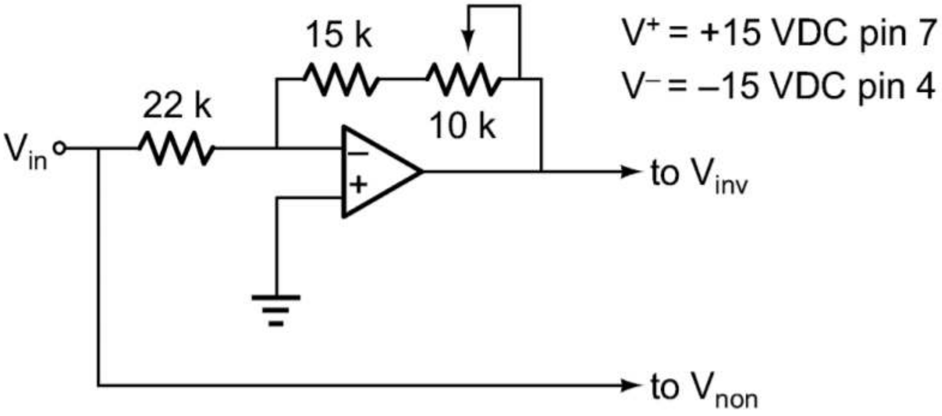

Figure 6.5.2

6.6: Procedure

1. This circuit can be examined through the use of the Superposition Theorem. The contribution of each input can be measured individually, combined, and then compared with common-mode and differential inputs.

2. Calculate the differential voltage gain for the amplifier and record it in Table 6.7.1

3. Assemble the circuit of Figure 6.5.1. Try to get the R_i/R_f ratio as close as possible to the R_i'/R_f' ratio, even if you have to mix and match several resistors.

4. Set the generator to a 1 kHz sine wave, 500 millivolts peak.

5. Apply the generator to the V_{inv} input, and ground the V_{non} input.

6. Measure and record the output voltage in Table 6.7.2, noting the phase relative to the input. Also, compute the resulting voltage gain.

7. Swap the inputs by connecting the V_{non} input to the generator, and grounding the V_{inv} input.

8. Measure and record the output voltage in Table 6.7.2, noting the phase relative to the input. Also, compute the resulting voltage gain.

9. Compare the results of step 6 to step 8. The gains should be identical except that one is inverting while the other is non-inverting. Calculate the results of adding the two output signals and place the values in Table 6.7.3.

10. To measure the common-mode gain, connect both inputs to the generator (removing the V_{inv} ground). Record the output voltage and resulting gain in Table 6.7.3.

11. Assemble the circuit of Figure 6.5.2. Adjust the potentiometer to set the voltage gain to precisely –1. This circuit is a simple phase-splitter and is used to generate a differential input signal.

12. Connect the circuit of Figure 6.5.2 to the original circuit as shown.

13. Measure and record the output voltage in Table 6.7.3.

14. Based on the results of Table 6.7.3, compute the experimental common-mode rejection ratio and place it in Table 6.7.4.

6.7: Data Tables

Theoretical Differential Gain	

Table 6.7.1

Input	V_{out}	Phase	A_v
V_{inv}			
V_{non}			

Table 6.7.1

Circuit	V_{out}	A_v
Superposition		
Common-mode		
Differential		

Table 6.7.1

Experimental CMRR	

Table 6.7.1

6.8: Questions

1. What controls the differential gain?

2. Why is it important to match the resistor ratios in step 3?

3. Why is it important to set the gain of the phase-splitter to precisely one in step 11?

4. What determines the theoretical maximum CMRR for the op amp differential amplifier?

CHAPTER OVERVIEW

7: Parallel-Series and Series-Series Negative Feedback

Objective

In this exercise, the performance of the current-source amplifiers will be examined. The investigation will include the effect of feedback resistors on setting gain for both the parallel-series inverting current amplifier and the series-series non-inverting voltage-to-current transducer.

7.1: Theory Overview

Series-output feedback connections create controlled current sources. This means that the load current will be constant in spite of changes in load impedance. Two variants are possible. Parallel-input connections create a current-sensing circuit, thus P-S feedback forms a current-controlled current-source, or ideal current amplifier. The current gain is set by the two feedback resistors, R_i and R_f. Series-input connections create a voltage-sensing circuit, thus S-S feedback forms a voltage-controlled current-source, or voltage-to-current transducer. The transconductance is set by the feedback resistor R_i.

7.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 3.4, The Four Variants of Negative Feedback

Section 4.2, Inverting and Non-inverting Amplifiers

7.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

7.4: Components

(1) General purpose op amp (741, 351, 411, 081, etc.)

(2) 1μ F

actual:____________________ ____________________

(1) 100 Ω

actual:____________________

(2) 1k Ω

actual:____________________ ____________________

(1) 2k2 Ω

actual:____________________

(1) 3k3 Ω

actual:____________________

(1) 4k7 Ω

actual:____________________

(2) 10k Ω

actual:____________________ ____________________

(2) 22k Ω

actual:____________________ ____________________

7.5: Schematics

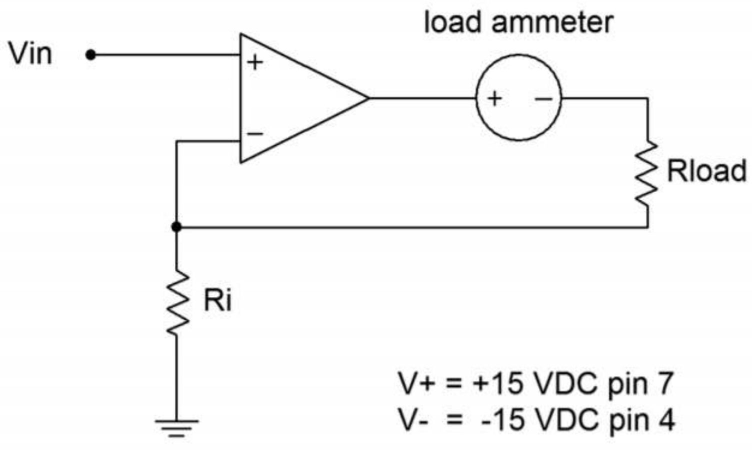

Figure 7.5.1

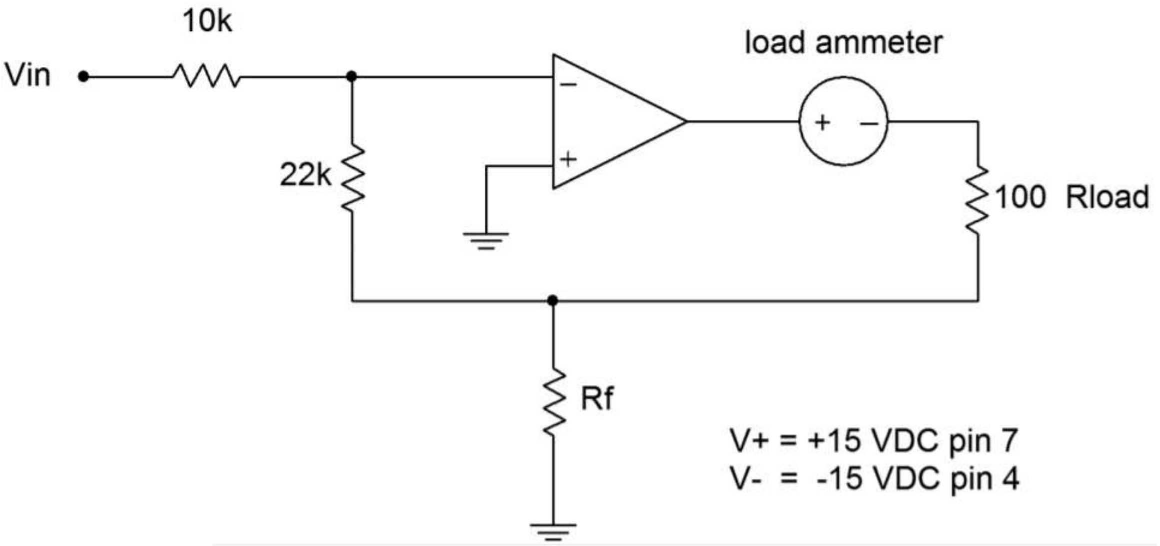

Figure 7.5.2

7.6: Procedure

7.6.1: Series-Series Voltage-to-Current Transducer

1. The transconductance of the voltage-to-current transducer can be determined from R_i. Based on the R_i values, calculate the expected I_{load} for the circuit of Figure 7.5.1, and record them in Table 7.7.1.

2. Assemble the circuit of Figure 7.5.1 using R_i = 1k Ω and R_{load} = 100 Ω.

3. Set the generator to a 100 Hz sine wave, 1 volt peak.

4. Apply the generator to the amplifier. Measure and record the load current in Table 7.7.1. Also, compute the resulting theoretical versus experimental deviation.

5. Repeat step 4 for the remaining R_i values in Table 7.7.1.

6. Since the circuit behaves as a constant current source, the value of the load resistance should have no effect on the load current (within normal parameters). To verify this, change R_{load} to 1k Ω and repeat steps 4 and 5, using Table 7.7.2.

7.6.2: Parallel-Series Current Amplifier

7. The gain of the current amplifier can be determined from R_i and R_f. Based on these values, calculate the expected A_i and I_{load} for the circuit of Figure 7.5.2, and record them in Table 7.7.3.

8. Assemble the circuit of Figure 7.5.2 using 22k Ω for R_f.

9. Set the generator to a 100 Hz sine wave, 1 volt peak. Note that the 10k Ω resistor at the input serves to convert the voltage from the generator into a current. With the values specified, the input current should be approximately 100 microamps.

10. Apply the generator to the amplifier. Measure and record the load current in Table 7.7.3. Also, compute the resulting current deviation.

11. Repeat step 10 for the remaining R_f values in Table 7.7.3.

7.6.3: Troubleshooting

12. Utilizing the circuit of Figure 7.5.2, suppose that all of the results found in Table 7.7.3 are approximately 10 times smaller than they should be. Consider and test at least two plausible causes for this scenario, and include the results in the technical report.

7.7: Data Tables

R_i	I_{load} 100 Ω Theory	I_{load} 100 Ω Experiment	% Deviation
1k Ω			
2k2 Ω			
3k3 Ω			
4k7 Ω			
10k Ω			

Table 7.7.1

R_i	I_{load} 1k Ω Theory	I_{load} 1k Ω Experiment	% Deviation
1k Ω			
2k2 Ω			
3k3 Ω			
4k7 Ω			
10k Ω			

Table 7.7.2

R_f	A_i Theory	I_{load} Theory	I_{load} Experiment	% Deviation
22k Ω				
10k Ω				
4k7 Ω				
2k2 Ω				

Table 7.7.3

7.8: Questions

1. What is the effect as R_i is increased in the circuit of Figure 7.5.1?

2. Does the load impedance play an appreciable role in setting the load current?

3. What is the effect as R_f is decreased in the circuit of Figure 7.5.2?

4. In practical voltage-source circuits, the load impedance can be too small, forcing the op amp into current limiting with resulting distortion. Are there similar limits in the current-source circuits?

CHAPTER OVERVIEW

8: Gain-Bandwidth Product

Objective

In this exercise, the upper frequency limit of a typical amplifier will be examined. The investigation will include the effect of voltage gain on f_2. Two different measurement techniques will be employed: direct measurement of the 3 dB frequency, and indirect measurement via rise time.

8.1: Theory Overview

The upper break frequency, f_2, of a typical amplifier is a function of the circuit gain and the op amp's unity-gain frequency, f_{unity}. Typical op amps exhibit a 20 dB per decade roll off slope in their open-loop response. When negative feedback is applied, this results in a direct tradeoff between closed-loop gain and f_2. Any increase in gain results in an equivalent decrease in f_2, and vice versa. In other words, the product of closed-loop gain and f_2 must be a constant. This constant can be found on a device data sheet as either f_{unity} or GBW (short for Gain-BandWidth product).

8.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 5.3, Gain-Bandwidth Product

8.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

8.4: Components

(1) Medium speed op amp (351, 411, 081, etc., do not use 741 or similar)

(2) 1μ F

actual:___________________ ___________________

(1) 220 Ω

actual:___________________

(1) 4k7 Ω

actual:___________________

(1) 10k Ω

actual:___________________

(1) 22k Ω

actual:___________________

(1) 33k Ω

actual:___________________

(1) 47k Ω

actual:___________________

8.5: Schematics

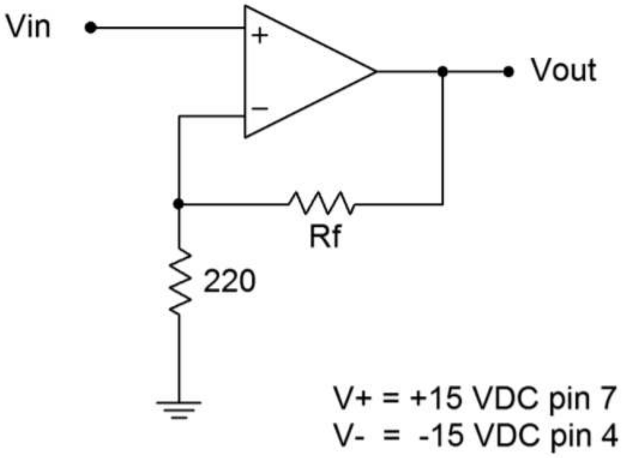

Figure 8.5.1

8.6: Procedure

1. The upper break frequency, f_2, of the amplifier in Figure 8.5.1 can be determined from its voltage gain and the f_{unity} of the op amp. Calculate the f_2 values for the amplifier of Figure 8.5.1 for the R_f values specified, and record them in Table 8.7.1.

2. Assemble the circuit of Figure 8.5.1 using the 4k7 Ω resistor.

3. Set the generator to a 100 Hz sine wave.

4. Apply the generator to the amplifier and adjust its level to achieve a 5 volt peak signal out of the op amp. Measure the input voltage and compute the resulting voltage gain. Record this voltage gain in Table 8.7.1.

5. Increase the frequency until the op amp's output voltage drops 3 dB (i.e., to 0.707 times 5 volts peak). Record this frequency in Table 8.7.1 as the experimental f_2.

6. Compute the experimental f_{unity} by multiplying the experimental voltage gain by the experimental f_2, and enter this value in Table 8.7.1.

7. Repeat steps 3 through 6 for the remaining R_f values in Table 8.7.1. Note that the values in the experimental f_{unity} column should be consistent with the f_{unity} specified in the device data sheet.

8. An alternate method to determine f_2 is to measure the rise time of an output square wave. To follow this method, first set the generator to a 1 kHz square wave.

9. Apply the generator to the amplifier and adjust its level to achieve a 2 volt peak signal out of the op amp. Measure the rise time and record this value in Table 8.7.2. An accurate measurement is important, so be sure to expand the time base so that the rising edge fills the majority of the oscilloscope display.

10. Use the rise time to compute the experimental f_2, and record this value in Table 8.7.2.

11. Compute the experimental f_{unity} by multiplying the experimental voltage gain from Table 8.7.1 by the experimental f_2 found in step 10, and enter this value in Table 8.7.2.

12. Repeat steps 9 through 11 for the remaining R_f values in Table 8.7.2. Note that the values in the experimental f_{unity} column should be consistent with those found in Table 8.7.1.

8.6.1: Computer Simulation

13. Build the circuit in a simulator and run an AC Analysis for each resistor listed in Table 8.7.1. Be sure to run the plot from 100 Hz to approximately f_{unity} and use a decibel scale for the gain amplitude. Record the simulation f_2 results in Table 8.7.3 and compare them to the f_2 values measured in Tables 8.7.1 and 8.7.2. Include the graph for the 4k7 with the technical report.

8.7: Data Tables

R_f	f_2 Theory	A_v Experiment	f_2 Experiment	f_{unity} Experiment
4k7 Ω				
10k Ω				
22k Ω				
33k Ω				
47k Ω				

Table 8.7.1

R_f	T_{rise} Experiment	f_2 Experiment	f_{unity} Experiment
4k7 Ω			
10k Ω			
22k Ω			
33k Ω			
47k Ω			

Table 8.7.2

R_f	f_2 Simulation
4k7 Ω	
10k Ω	
22k Ω	
33k Ω	
47k Ω	

Table \(\PageIndex{3}\)

8.8: Questions

1. What is the effect on f_2 as A_v is increased?

2. What is the effect on rise time as A_v is increased?

3. Is f_{unity} a constant across a wide range of voltage gains?

4. How would the results of this exercise differ if an op amp with a considerably higher f_{unity} was used?

CHAPTER OVERVIEW

9: Slew Rate and Power Bandwidth

Objective

In this exercise, the effects of slew rate on pulse and sinusoidal waveforms will be examined.

9.1: Theory Overview

Slew rate places an upper "speed limit" on the rate of change of output voltage. This tends to slow the rising and falling edges of pulse signals, turning them into a trapezoidal shape. In the case of sinusoidal signals, slew rate limiting tends to turn waves into a more triangular shape. The maximum non-slewed sine wave frequency for a given output amplitude is termed the power bandwidth, or f_{max}. Any output signal that exceeds the power bandwidth at the stated output amplitude will exhibit slew rate induced distortion. Slew rate is determined by the internal characteristics of a given op amp. In most op amps, circuit gain or feedback resistor values do not affect the slew rate.

9.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 5.4, Slew Rate and Power Bandwidth

9.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

9.4: Components

(3) General purpose op amps (1 each of 741, 351, 081, 411, etc., do not use 318 or similar)

(2) 1μ F

actual:___________________ ___________________

(1) 2k2 Ω

actual:___________________

(1) 10k Ω

actual:___________________

(1) 22k Ω

actual:___________________

(1) 33k Ω

actual:___________________

(1) 47k Ω

actual:___________________

9.5: Schematics

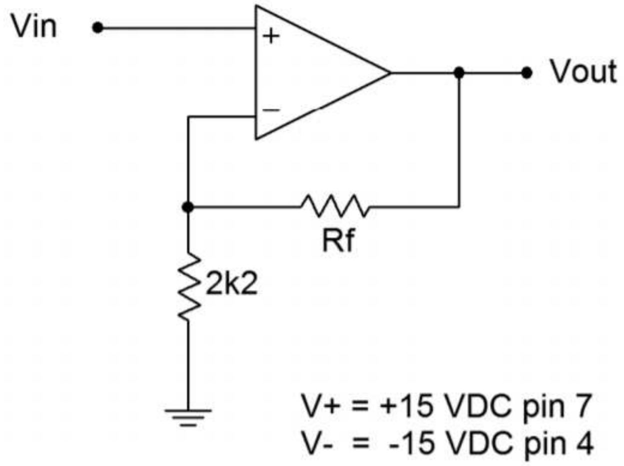

Figure 9.5.1

9.6: Procedure

1. Calculate the voltage gains for the amplifier of Figure 9.5.1 for the R_f values specified, and record them in Table 9.7.1.

2. Look up the typical slew rates for the three op amps and place them in Table 9.7.2.

3. Assemble the circuit of Figure 9.5.1 using the 22k Ω resistor and the slowest op amp.

4. Set the generator to a 1 kHz square wave.

5. Apply the generator to the amplifier and adjust the generator's amplitude to achieve a clipped signal at the output of the op amp. Make sure that the edges of the waveform are sharp, and not rounded. Expand the time scale so that the rising edge fills the oscilloscope display. Measure and record the slew rate in Table 9.7.1.

6. Repeat step 5 for the remaining R_f values in Table 9.7.1.

7. Set R_f to 10k Ω. Set the generator to a 1 kHz square wave.

8. Apply the generator to the amplifier and adjust the generator's amplitude to achieve a clipped signal at the output of the op amp. Save a copy of the oscilloscope display showing approximately one cycle of the waveform. Measure and record the slew rate in Table 9.7.2.

9. Repeat step 8 for the other op amps in Table 9.7.2.

10. Using a peak sine wave output of 10 volts, compute the theoretical power bandwidth for each of the op amps in Table 9.7.3.

11. Set the generator to a 1 kHz sine wave.

12. Apply the generator to the amplifier and adjust the generator's amplitude to achieve a 10 volt peak signal at the output of the op amp.

13. While monitoring the amplifier's output signal with the oscilloscope, increase the frequency until slew rate limiting occurs (the waveform will start to appear triangular). The point at which slew rate limiting just begins is not easy to discern by eye. If the waveform is triangular, then the op amp is well into slew rate limiting. Gradually decrease the frequency until the waveform distortion just seems to disappear. Record the frequency as the experimental f_{max} in Table 9.7.3.

14. Repeat steps 11 through 13 for the remaining op amps in Table 9.7.3.

9.6.1: Computer Simulation

15. Build the circuit in a simulator and run a Transient Analysis for each op amp used in Table 9.7.2, echoing steps 7 through 9. Be sure to set the time scale so that at least one but no more than two cycles are plotted. Compare these to the corresponding oscilloscope images and include the graphs with the technical report.

9.7: Data Tables

R_f	A_v Theory	Slew Rate Experiment
22k Ω		
33k Ω		
47k Ω		

Table $9.7.1$

Op Amp	Slew Rate Theory	Slew Rate Experiment
1		
2		
3		

Table $9.7.2$

Op Amp	f_{max} Theory	f_{max} Experiment	% Deviation
1			
2			
3			

Table $9.7.3$

9.8: Questions

1. Does voltage gain affect slew rate?

2. How does the slew rate affect power bandwidth?

3. How does the output amplitude affect power bandwidth?

4. Is it possible for triangle waves to suffer from slew rate limiting?

CHAPTER OVERVIEW

10: The Non-compensated Op Amp

Objective

In this exercise, the performance of a typical non-compensated op amp, the 301, will be examined. The investigation will include the effect of the external compensation capacitor on voltage gain, closed-loop bandwidth and slew rate.

10.1: Theory Overview

Op amps usually contain an internal compensation capacitor, C_c. This capacitor enforces a 20 dB per decade gain slope up to the unity-gain frequency, and allows stable voltage gains down to unity. Unfortunately, this will not normally produce optimal values for small signal bandwidth and slew rate for gains considerably greater than unity. In the case where unity-gain stability is not required, a smaller value for C_c may be used, resulting in improved bandwidth and slew rate. Non-compensated op amps include connections for an external compensation capacitor that can be adjusted for optimal performance.

10.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 5.4, Slew Rate and Power Bandwidth

10.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) DMM capable of measuring in dB

model:_________________ srn:___________________

10.4: Components

(1) LM301 op amp

(2) 1 μF actual:____________________ ____________________

(1) 150 pF actual:____________________

(1) 33 pF actual:____________________

(1) 10 pF actual:____________________

(1) 22 kΩ actual:____________________

(1) 47 kΩ actual:____________________

(1) 100 kΩ actual:____________________

LM301 Data sheet: http://www.ti.com/lit/ds/symlink/lm101a-n.pdf

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10.5: Schematics

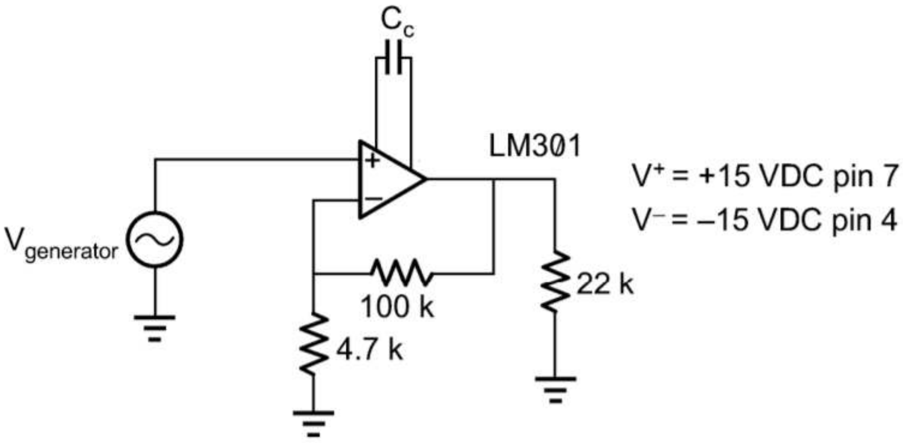

Figure 10.5.1

10.6: Procedure

1. Notice that Figure 10.5.1 is a series-parallel non-inverting voltage amplifier. Calculate the theoretical voltage gain for the amplifier and record it in Table 10.7.1.

2. Assemble the circuit using C_c = 150 pF.

3. Set the generator to a 100 Hz sine wave.

4. Set the output voltage of the op amp to 1 volt peak. Measure and record the input voltage in Table 10.7.2. Also, compute the resulting voltage gain.

5. Using the decibel-reading voltmeter, increase the input frequency until the op amp's output voltage drops 3 dB from it's value at 100 Hz. If a dB meter is not available, use the oscilloscope to find the frequency at which the op amp's output voltage drops to 0.707 times the 100 Hz value. (Note that –3 dB corresponds to a factor of 0.707.) Record the frequency in Table 10.7.2.

6. Change the generator to a 10 kHz square wave.

7. Increase the generator's amplitude so that the output of the op amp is obviously slewed, about 10 volts peak (straight lines for the leading and trailing edges).

8. Measure the slew rate and record it in Table 10.7.2.

9. Repeat steps 3 through 8 using C_c = 33 pF and C_c = 10 pF.

10.7: Data Tables

Theoretical voltage gain	

Table 10.7.1

C_c	V_{in}	A_v	f_2	SR
150 pF				
33 pF				
10 pF				

Table 10.7.2

10.8: Questions

1. How does f_2 vary with C_c?

2. How does A_v vary with C_c?

3. How does slew rate vary with C_c?

4. What is the effect on small signal bandwidth and power bandwidth as C_c is decreased?

5. How does this op amp compare with a typical compensated op amp such as the 741?

CHAPTER OVERVIEW

11: DC Offset

Objective

In this exercise, the effect of DC offsets will be examined. The investigation will include the effect of voltage gain and op amp on the magnitude of offset, as well as standard techniques to null or remove offsets.

11.1: Theory Overview

A DC offset is an undesirable effect. Due to internal mismatches in the op amp, a DC signal may be present at the output of an amplifier. This generally does not present a problem for an AC amplifier, but it does lead to ambiguity in the output of a DC amplifier. A DC offset may be either positive or negative. The magnitude of the offset is proportional to the gain of the amplifier and the size of the feedback resistors. It also depends on the "luck of the draw," in other words, just how well matched the internals of a given op amp happen to be.

11.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 5.5, Offsets

11.3: Equipment

(1) Dual DC power supply

model:________________ srn:__________________

(1) DMM

model:________________ srn:__________________

11.4: Components

(2) General purpose op amps (741, 351, 081, etc., do not use 411 or similar precision device)

(2) 1μ F

actual:___________________ ___________________

(2) 1k Ω

actual:___________________ ___________________

(1) 4k7 Ω

actual:___________________

(1) 10k Ω

actual:___________________

(1) 22k Ω

actual:___________________

(1) 33k Ω

actual:___________________

(1) 47k Ω

actual:___________________

(1) 10k Ω potentiometer

11.5: Schematics

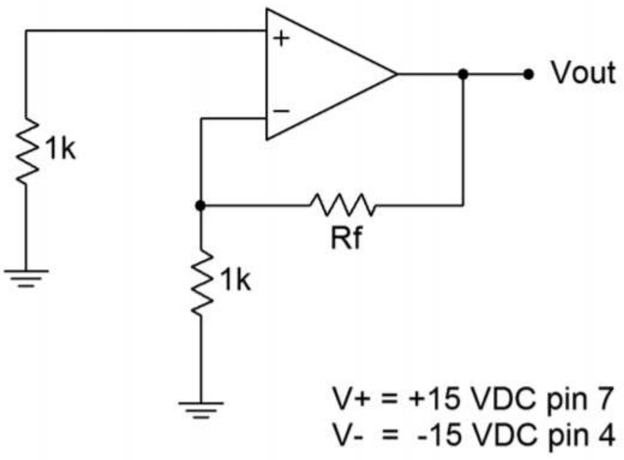

Figure 11.5.1

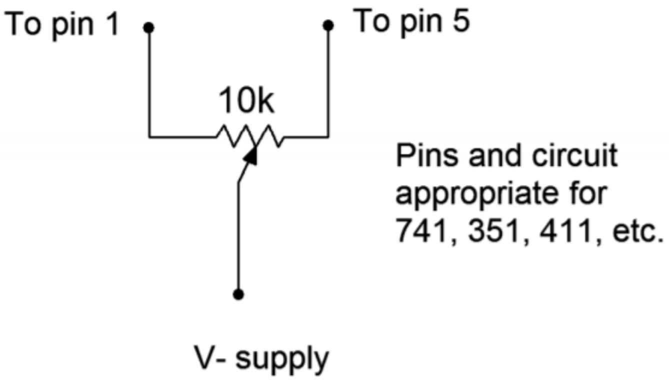

Figure 11.5.2

11.6: Procedure

1. Note that the circuit of Figure 11.5.1 is a non-inverting voltage amplifier. Calculate the voltage gains for the amplifier of Figure 11.5.1 for the R_f values specified, and record them in Table 11.7.1.

2. The worst case output offset may be approximated by multiplying the worst case V_{os} found in the op amp’s data sheet by the voltage gain. This ignores the effect of the feedback resistor values. Calculate the offsets for the gains found in step 1, and record the values in Table 11.7.1.

3. Assemble the circuit of Figure 11.5.1 using the 4k7 Ω resistor.

4. Measure and record the DC output offset voltage in Table 11.7.1.

5. Repeat step 4 for the remaining R_f values in Table 11.7.1.

6. Compute the resulting experimental V_{os} values by dividing the output offsets by the corresponding voltage gains. The experimental V_{os} values should be no larger than the value specified in the data sheet, although they may be considerably smaller. Finally, compute the offset deviations. Note that the V_{os} and deviation values should be fairly constant through the table.

7. Since the actual V_{os} of any given op amp can range between +/– V_{os} worst case, a different device may produce considerably different values from those in Table 11.7.1. To verify this, repeat steps 3 through 6 for a second op amp, and record your results in Table 11.7.2.

8. Manufacturers normally allow for output nulling through the addition of external circuitry. Modify the circuit by adding the components shown in Figure 11.5.2. Using the 47k Ω resistor for Rf, adjust the potentiometer to null the output. Also, record the DC output voltage with the potentiometer fully clockwise and fully counterclockwise.

11.6.1: Computer Simulation

9. Build the circuit of Figure 11.5.1 in a simulator using a 741 op amp and 47k for R_f. Run a DC Operating Point analysis to determine the DC output voltage. Compare this to the results measured in Tables 11.7.1 and 11.7.2. Repeat the simulation with all resistors 10 times larger, and again with all resistors 100 times larger.

11.7: Data Tables

R_f	A_v Theory	V_{out} Theory	V_{out} Experiment	V_{os} Experiment	% Deviation
4k7 Ω					
10k Ω					
22k Ω					
33k Ω					
47k Ω					

Table 11.7.1

R_f	A_v Theory	V_{out} Theory	V_{out} Experiment	V_{os} Experiment	% Deviation
4k7 Ω					
10k Ω					
22k Ω					
33k Ω					
47k Ω					

Table 11.7.2

Potentiometer	V_{out}
CW	
CCW	

Table 11.7.3

11.8: Questions

1. What is the effect on output offset voltage as the voltage gain is increased?

2. Is the worst case V_{os} a good approximation for the actual V_{os}? Explain.

3. Given the range of adjustment found in Table 11.7.3 along with the data from Tables 11.7.1 and 11.7.2, is it likely that the circuitry of Figure 11.5.1 will be sufficient to correct for the offset produced by a worst case op amp? Explain.

4. Based on the simulation results, is it safe to say that output DC offset is only affected by voltage gain and not the specific feedback resistor values used?

CHAPTER OVERVIEW

12: The Operational Transconductance Amplifier

Objective

In this exercise, an application of the operational transconductance amplifier (OTA) will be examined. The application is that of a voltage-controlled amplifier (VCA). The VCA has use in a variety of areas including automatic gain control, audio level compressors and amplitude modulators.

12.1: Theory Overview

The gain of the OTA is a function of a programming current, I_{abc}. Since I_{abc} may be derived from other electronic signals, complex dynamic gains are possible. Further, because the OTA tends to behave as an ideal current source (i.e., it exhibits a high output impedance), a constant voltage output is best rendered through the use of a following current-to-voltage transducer. Finally, the OTA can only tolerate fairly small input signals, so some form of input attenuation is normally used.

12.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 6.7, Operational Transconductance Amplifier

12.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(2) Function generators

model:_________________ srn:___________________

model:_________________ srn:___________________

(1) Triple DC power supply

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

12.4: Components

(1) 3080 OTA (or 13600 or 13700 with alternate pin-out)

(1) FET input op amp (351, 411, 081, etc.)

(2) 1 μF

actual:___________________ ___________________

(2) 470 Ω

actual:___________________ ___________________

(2) 22 kΩ

actual:___________________ ___________________

(1) 33 kΩ

actual:___________________

(2) 47 kΩ

actual:___________________ ___________________

(1) 100 kΩ

actual:___________________

(1) 10 kΩ potentiometer

LM3080 Data sheet: www.ti.com/lit/ds/symlink/lm3080.pdf

LM13700 Data sheet: http://www.ti.com/lit/ds/symlink/lm13700.pdf

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12.5: Schematics

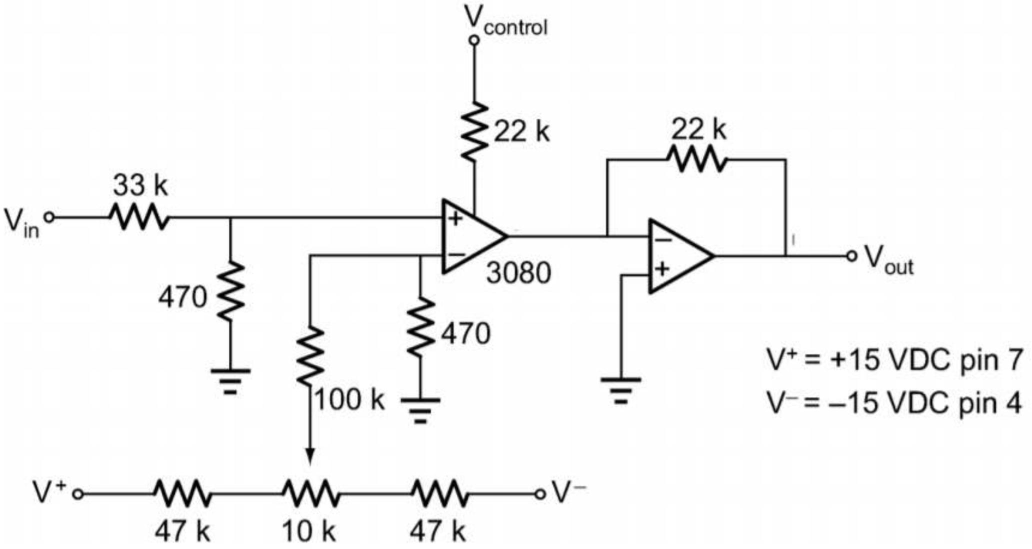

Figure 12.5.1

12.6: Procedure

1. Assemble the circuit of Figure 12.5.1 . Note that the power supplies are only +/– 5 VDC, not the usual +/– 15 VDC.

2. For proper operation, it is very important that any DC input signals be nulled. Failure to do so will cause the control signal to "leak" into the output. To null the circuit, first tie the left end of the 33 kΩ resistor to ground. Also, tie $V_{control}$ to ground. Finally, adjust the potentiometer until V_{out} is 0 VDC. The circuit is now nulled. Unhook the resistor and control points from ground in order to continue to the next step.

3. Set $V_{control}$ to –3 VDC. If a third output is not available on the DC power supply, the –3 VDC potential may be derived from the –5 VDC supply and appropriate divider resistors.

4. Set the main generator to a 100 kHz sine wave, 1 volt peak.

5. Apply the generator to the circuit input. Measure and record the output voltage in Table 12.7.1. Also, compute the resulting experimental voltage gain.

6. Repeat steps 3 through 5 for the remaining $V_{control}$ values in Table 12.7.1 .

7. Using the data from Table 12.7.1, plot the gain versus control voltage characteristic as Graph 1.

8. Set the second generator to a 1 kHz sine wave, 1 volt peak. Apply the second generator to the $V_{control}$ point.

9. Set the main generator to a 1 volt peak 100 kHz sine wave, and connect it to the circuit input.

10. Measure and record the output waveform as Graph 2.

11. Change the main generator to a 1 volt peak 100 kHz triangle wave and record the resulting output waveform as Graph 3.

12.7: Data Tables

$V_{control}$	V_{out}	A_v
–3 VDC		
–2 VDC		
–1 VDC		
0 VDC		
+1 VDC		
+2 VDC		
+3 VDC		

Table $12.7.1$

12.8: Questions

1. What is the effect as $V_{control}$ is increased?

2. Is the control/gain relationship linear?

3. What is the purpose of the second op amp in Figure 12.5.1?

4. Explain how the control signal “leaks” into the output signal if the circuit is not nulled properly.

5. Based on Graphs 2 and 3, does this circuit appear to be a good candidate for an amplitude modulator?

CHAPTER OVERVIEW

13: Precision Rectifiers

Objective

In this exercise, precision half-wave and full-wave rectifiers will be examined. The investigation will include the accuracy of rectification and peak detection.

13.1: Theory Overview

Simple passive diode circuits cannot rectify small signals accurately. The forward bias potential of the diode acts as a constant barrier. By placing the diode inside the feedback loop of an op amp, the forward bias potential can be compensated for to a great extent. Both half-wave and full-wave circuits can be created in this fashion. Further, the addition of load capacitance can be used to create a simple envelope detector. On the downside, the frequency response of precision rectifiers is limited by the op amp(s) used.

13.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 7.2, Precision Rectifiers

13.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

13.4: Components

(2) General purpose op amps (741, 351, 411, 081, etc.)

(2) Small-signal diodes (1N914, 1N4148, etc.)

(3) 1μ F

actual:____________________ ____________________ ____________________

(1) 10n F

actual:____________________

(1) 22k Ω

actual:____________________

(6) Equal value resistors in the range of 10k Ω to 100k Ω

actual:____________________ ____________________ ____________________

actual:____________________ ____________________ ____________________

1N4148/1N914 Datasheet: https://www.onsemi.com/pub/Collateral/1N914-D.PDF

13.5: Schematics

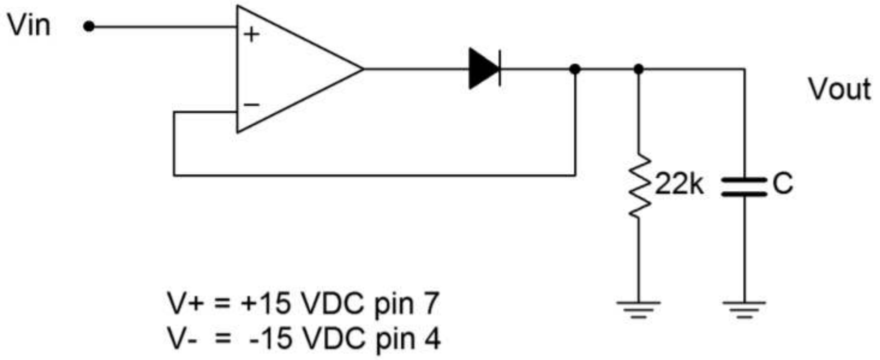

Figure 13.5.1

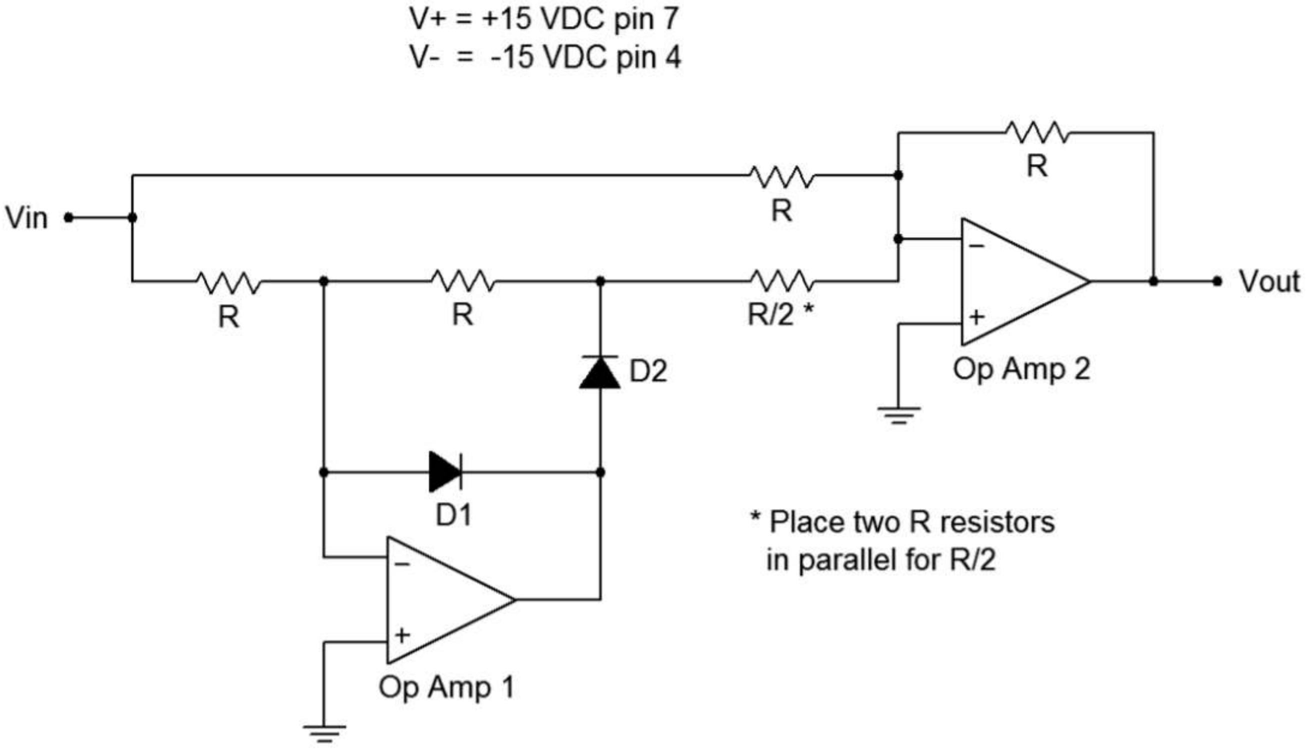

Figure 13.5.2

13.6: Procedure

13.6.1: Precision Half-wave Rectifier and Detector

1. The circuit of Figure 13.5.1 is a precision half-wave rectifier. Without C, the circuit responds as an “ideal diode” allowing only positive half-waves through. The addition of C turns the circuit into peak detector or analog pulse-stretcher. Since all of the circuits in this exercise can produce DC components in the output signals, it is very important to take measurements with the oscilloscope input set to DC coupled.

2. Assemble the circuit of Figure 13.5.1 without the load capacitor.

3. Set the generator to a 1 kHz sine wave, and set its output voltage to 1 volt peak.

4. Measure V_{out} and save a copy of the oscilloscope display as Graph 1. Also measure and save the waveform at the output pin of the op amp as Graph 2.

5. Reverse the diode, measure V_{out} and save a copy of the oscilloscope display as Graph 3.

6. While monitoring the load voltage, increase the frequency of the generator and note how the distortion in the waveform increases. If a considerably faster or slower op amp is available (in terms of f_{unity} and slew rate), repeat this process and compare the frequencies at which the two op amps start to distort.

7. Return the diode to its original orientation and add C = 10n F.

8. Apply a 1 volt peak 1 kHz pulse waveform with 10% duty cycle to the input of the circuit.

9. Measure V_{out} and save a copy of the oscilloscope display as Graph 4.

10. Replace the 10n F load capacitor with a 1μ F capacitor. Measure and save the V_{out} waveform as Graph 5.

13.6.2: Precision Full-wave Rectifier

11. Decide on a value for R in Figure 13.5.2 and assemble it. The actual value of R is not critical. The important thing is that the resistors should be close in value, preferably within a few percent of each other.

12. Set the generator to a 1 kHz sine wave, and set its output voltage to 1 volt peak.

13. Record the waveforms at the cathode of D_2 and at V_{out} as Graph 6.

14. Reverse the polarity of the diodes and record the waveforms at D_2 and at V_{out} as Graph 7.

15. Try several different input wave shapes (square, triangle, ramp, etc.) while monitoring V_{out} and note the resulting shapes.

16. Set the generator to a 1 volt peak 100 Hz sine wave and place the oscilloscope in XY mode.

17. For Graph 8, plot the transfer characteristic of the circuit by placing the X (horizontal) probe at the generator, and the Y (vertical) probe at the load (V_{out}).

13.6.3: Troubleshooting

18. Continuing with the circuit of Figure 13.5.2, estimate and then measure the results for each individual error presented in Table 13.7.1.

13.6.4: Computer Simulation

19. Build the circuit of Figure 13.5.1 in a simulator using a 351 op amp and without the load capacitor. Run a Transient Analysis to determine the voltages at the output pin of the op amp and at V_{out}. Compare the waveforms to those recorded as Graphs 1 and 2.

13.7: Data Tables

Error	Quantity	Estimate	Actual
$R/2$ is simply R	V_{out}		
D_2 is shorted	V_{out}		
R_i of op amp 1 is open	V_{out}		

Table $13.7.1$

13.8: Questions

1. What is the effect of flipping the diode in Figure 13.5.1?
2. How does the output waveform of the op amp itself compare with the load waveform?
3. What is the effect of increasing load capacitance in Figure 13.5.1?
4. In general, what can be said about the use of op amps with high slew rates and f_{unity} values in precision rectifiers?
5. What is the effect of flipping the diodes in Figure 13.5.2?
6. Briefly describe what each half of Figure 13.5.2 is doing.
7. What would be the effect of doubling R_f of the second op amp of Figure 13.5.2?

CHAPTER OVERVIEW

14: Function Generation

Objective

In this exercise, the concept of function generation will be examined. The investigation will include the use of both biased diode networks and Zener diodes. Increasing as well as decreasing gain curves will be used.

14.1: Theory Overview

The gain of an amplifier can be nonlinear if the feedback resistors themselves are nonlinear. By shunting feedback resistors with resistor-diode networks, the effective feedback resistance decreases as the input signal increases. If this network is placed across R_i, then an increasing gain function will be created. If the network is placed across R_f, then a decreasing gain function will be created. By combining several resistor-diode sections, complex transfer curves can be created.

14.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 7.4, Function Generation

14.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

14.4: Components

(1) General purpose op amp (741, 351, 411, 081, etc.)

(2) General purpose switching diodes (1N914, 1N4148, etc.)

(2) 5.1 volt Zener diodes (NZX5V1B or 1N5231)

(2) 3.3 volt Zener diodes (NZX3V3B or 1N5226)

(2) 1μ F

actual:____________________ ____________________

(1) 4k7 Ω

actual:____________________

(2) 10k Ω

actual:____________________ ____________________

(1) 12k Ω

actual:____________________

(1) 15k Ω

actual:____________________

(1) 22k Ω

actual:____________________

(1) 33k Ω

actual:____________________

(1) 47k Ω

actual:____________________

(1) 56 kΩ

actual:____________________

1N4148/1N914 Datasheet: https://www.onsemi.com/pub/Collateral/1N914-D.PDF

NZX Series Datasheet: https://assets.nexperia.com/document...et/NZX_SER.pdf

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14.5: Schematics

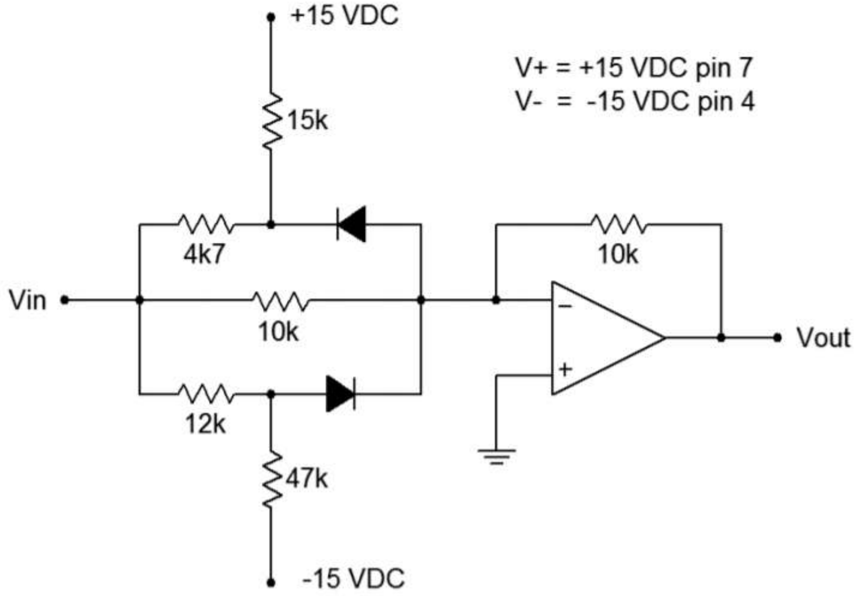

Figure 14.5.1

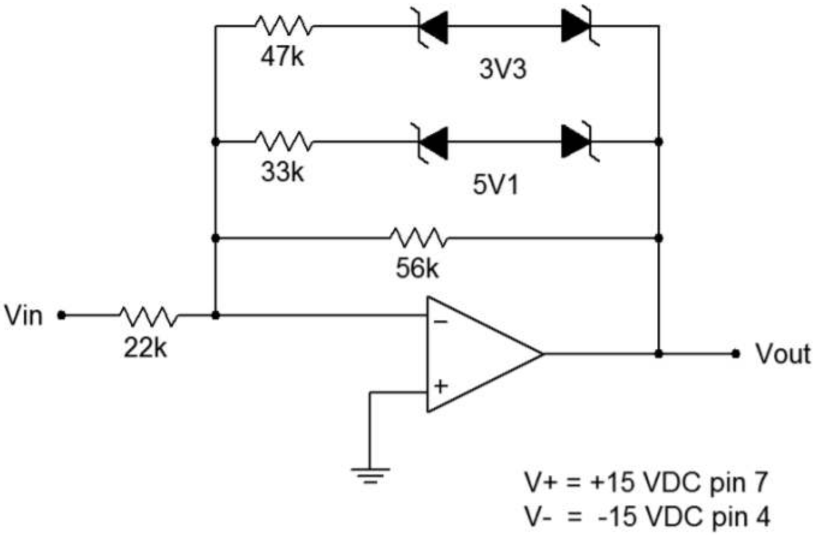

Figure 14.5.2

14.6: Procedure

14.6.1: Biased Diode Network

1. Calculate the break-points and slopes for the input/output transfer curve of the circuit in Figure 14.5.1. Record these values in Table 14.7.1.

2. Assemble the circuit of Figure 14.5.1.

3. Set the generator to a 1 volt peak 100 Hz triangle wave.

4. While monitoring the output of the op amp, increase the amplitude of the triangle wave and note how the shape of the wave changes. Save the display of the output voltage as Graph 1.

5. Switch the oscilloscope to XY mode. Switch the inputs to ground in order to center the spot. Connect the input voltage to the X (horizontal) channel, and the output of the op amp to the Y (vertical) channel.

6. Switch the input channels to DC Coupled. Save the resulting input/output transfer curve as Graph 2.

14.6.2: Zener Diode Network

7. Calculate the break-points and slopes for the input/output transfer curve of the circuit in Figure 14.5.2. Record these values in Table 14.7.2.

8. Assemble the circuit of Figure 14.5.2.

9. Switch the oscilloscope back to Volts vs. Time mode.

10. Repeat steps 3 through 6, saving the displays as Graphs 3 and 4, respectively.

14.6.3: Troubleshooting

11. Continuing with the circuit of Figure 14.5.2, estimate and then measure the results for each individual error presented in Table 14.7.3.

14.7: Data Tables

Base voltage gain	
Positive break-point	
Gain beyond positive break-point	
Negative break-point	
Gain beyond negative break-point	

Table 14.7.1

Base voltage gain	
First break-point	
Gain beyond first break-point	
Second break-point	
Gain beyond second break-point	

Table 14.7.2

Error	Quantity	Estimate	Actual
33k swapped with 47k	V_{out}		
22k swapped with 56k	V_{out}		
One 5V1 Zener backwards	V_{out}		

Table 14.7.3

14.8: Questions

1. What would happen in Figure 14.5.1 if the 12k Ω and 4k7 Ω were swapped?

2. What happens in Figure 14.5.2 when the 33k Ω and 47k Ω are swapped?

3. Does the value of the DC power supply have any effect on the break-points of the circuit of Figure 14.5.1?

4. What is the effect of increasing the 22k Ω in Figure 14.5.2?

5. What would the transfer curve look like if Figures 14.5.1 and 14.5.2 were cascaded?

CHAPTER OVERVIEW

15: The Linear Regulator

Objective

In this exercise, the performance of a simple op amp-based linear regulator will be examined. The investigation will include the effect of scaling resistors on the load voltage and the usage of a current pass transistor.

15.1: Theory Overview

Regulators are used to create a stable, clean DC voltage to power other electronic systems. The regulator voltage should not change as its load changes. A linear regulator may be based on a series-parallel feedback loop, using an op amp as a controller. The op amp compares a scaled version of the load voltage to a reference voltage. By changing either the reference or the scaling factor, a range of load voltages may be obtained. Because op amps typically produce insufficient current to drive many loads, a current pass transistor is used to boost output current capability.

15.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 8.3, Linear Regulators

15.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Adjustable DC power supply

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

15.4: Components

(1) General purpose op amp (741, 351, 411, 081, etc.)

(1) Medium power NPN transistor (2N5190G-2N5192G)

(1) Zener diode around 5.1 volts (NZX5V1B, 1N751)

(2) 1μ F

actual:___________________ ___________________

(1) 2k2 Ω

actual:___________________

(2) 47k Ω

actual:___________________ ___________________

(2) 100k Ω

actual:___________________ ___________________

(1) 100 Ω 5 watt

actual:___________________

2N5192G Datasheet: www.onsemi.com/pub_link/Colla...l/2N5191-D.PDF

NZX5V1B Datasheet: https://assets.nexperia.com/document...et/NZX_SER.pdf

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15.5: Schematics

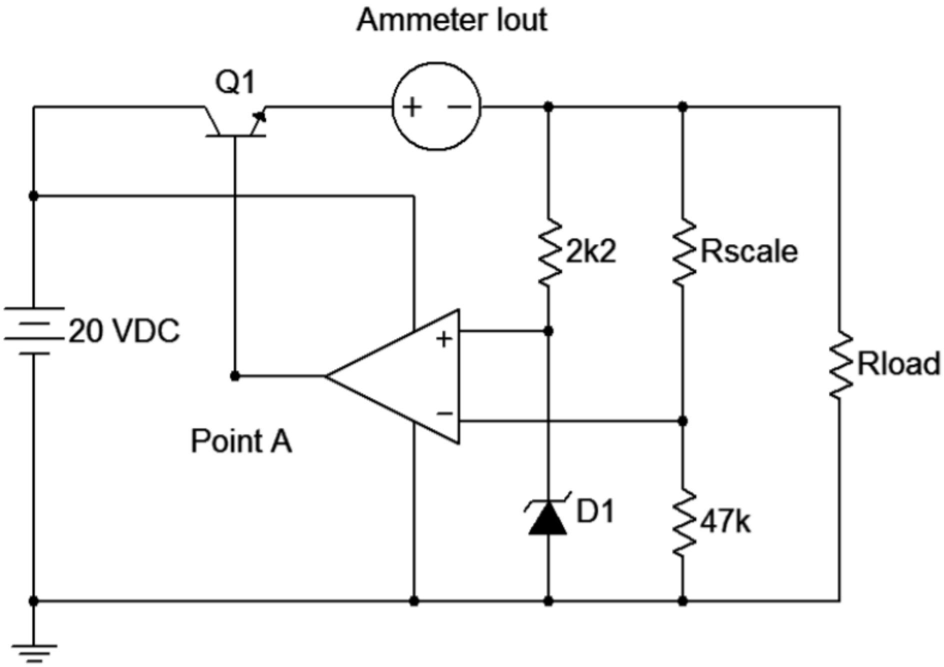

Figure 15.5.1

15.6: Procedure

1. In this exercise, a DC source is being used to simulate the output of a rectified and filtered power source in the interest of simplicity.

2. Note that the op amp is acting as a series-parallel feedback amplifier where the load voltage is equal to $V_{Zener}(1+R_{scale}/47\text{k }\Omega)$. Changes to the load resistor should cause no change in the load voltage. Also, note that I_{out} is equal to the transistor's β times the output current of the op amp. The transistor is therefore being used as a current booster, and because it is located inside of the feedback loop, it should not affect the load voltage.

3. Connect the circuit of Figure 15.5.1 using an R_{scale} of 47k Ω, and an R_{load} of 100k Ω.

4. Calculate and record the values for V_{load}, I_{load}, I_{out}, and $I_{out-op-amp}$ in Table 15.7.1. A typical β would be in the range of 50 to 100, depending on the pass transistor used.

5. Measure and record the values for V_{load}, I_{load}, I_{out}, and $I_{out-op-amp}$ (i.e., at point A) in Table 15.7.2.

6. Change R_{scale} to 100k Ω and repeat steps 4 and 5.

7. Change R_{scale} back to 47k Ω, change R_{load} to 100 Ω and repeat steps 4, 5, and 6.

15.6.1: Computer Simulation

8. One limitation of the preceding exercise is that it does not show how well the regulator suppresses AC ripple that might exist on the input power source. This can be accomplished easily in a simulator. Build the circuit in a simulator using R_{load} equal to 100 Ω and R_{scale} equal to 100k Ω. To create the ripple, simply insert an AC power source in series with the 20 volt DC source (i.e., inserted between ground and the negative terminal of the 20 volt source). Set the AC source to 120 Hz and 2 volts peak. This will mimic filtered full-wave rectified 60 Hz power ripple. Run a Transient Analysis to determine the load voltage. In the technical report, include a plot of the simulated load voltage along with the voltage applied to the collector of the pass transistor.

15.7: Data Tables

R_{load}	R_{scale}	V_{load}	I_{load}	I_{out}	$I_{out-op-amp}$
100k Ω	47k Ω				
100k Ω	100kΩ				
100 Ω	47k Ω				
100 Ω	100k Ω				

Table 15.7.1 (Theoretical)

R_{load}	R_{scale}	V_{load}	I_{load}	I_{out}	$I_{out-op-amp}$
100k Ω	47k Ω				
100k Ω	100kΩ				
100 Ω	47k Ω				
100 Ω	100k Ω				

Table 15.7.2 (Experimental)

15.8: Questions

1. How do the load voltage and current vary with the scale resistor?

2. How do the load voltage and current vary with the load resistor?

3. What is the relationship between I_{out} and $I_{out-op-amp}$?

4. What is the relationship between I_{out} and I_{load}?

5. How could this circuit be modified to produce a load voltage of 12 volts?

6. What is the maximum load current that can be obtained without damage to any of the devices?

CHAPTER OVERVIEW

16: The Triangle-Square Generator

Objective

In this exercise, a simultaneous triangle-square wave generator is examined. The investigation will include the effect of capacitance on output frequency, and the role of op amp speed in determining ideal wave shapes.

16.1: Theory Overview

The triangle-square generator consists of two main parts: a comparator and a ramp generator or integrator. The circuit is self-sustaining by nature. The ramp generator requires a square wave input. It gets this signal from the comparator. The comparator in turn generates the square wave from the triangle wave appearing at the output of the ramp generator. The output frequency is determined primarily by the RC timing values of the ramp generator, and secondarily by the switching thresholds of the comparator. The practical output frequency limit is set by the bandwidth and slew rate of the op amps. At higher frequencies, slew rate limiting will noticeably slow the edges of the square wave. This will impact the output of the ramp generator and will affect both the linearity of the wave shapes and the output frequency.

16.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 9.2, Op Amp Oscillators

16.3: Equipment

(1) Oscilloscope

model:__________________ srn:____________________

(1) Dual DC power supply

model:__________________ srn:____________________

(1) DMM

model:__________________ srn:____________________

16.4: Components

(2) Low speed op amps (741)

(2) Medium speed op amps (351, 411, 081, etc.)

(2) 1μ F

actual:____________________ ____________________

(1) 1n F

actual:____________________

(1) 10n F

actual:____________________

(1) 10k Ω

actual:____________________

(1) 22k Ω

actual:____________________

(1) 33k Ω

actual:____________________

16.5: Schematics

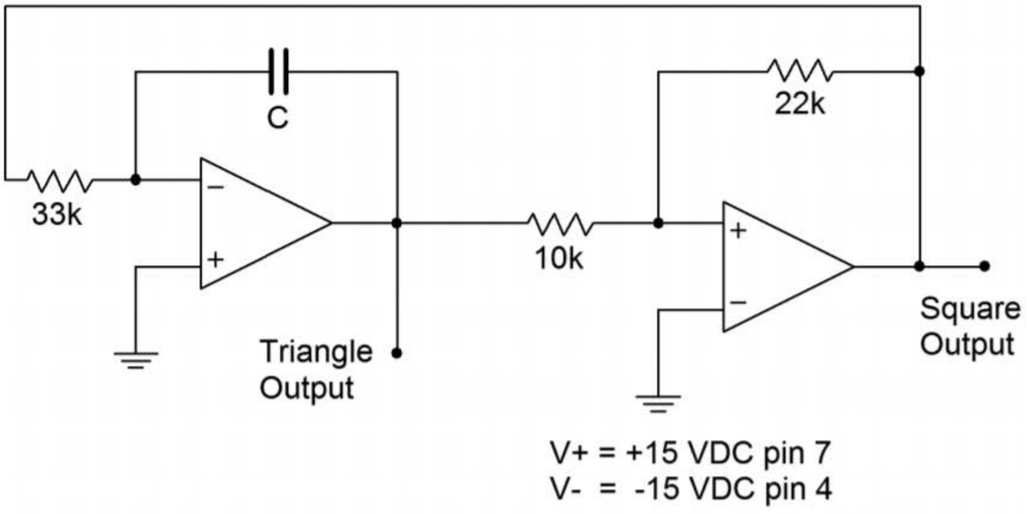

Figure 16.5.1

16.6: Procedure

1. Using 10n F for the capacitor, determine the theoretical output frequency and the peak value of the triangle wave. Record these items in Table 16.7.1.

2. Construct the circuit of Figure 16.5.1 using the 10n F capacitor and the medium speed op amps.

3. Record the output frequency and amplitude of the triangle wave in Table 16.7.1 and determine the deviation between the theoretical and experimental results.

4. Save a copy of the oscilloscope displaying the triangle and square waves as Graph 1.

5. Replace the capacitor with the 1n F unit. Determine the theoretical output frequency and the peak value of the triangle wave using this new value, and record the results in Table 16.7.2.

6. Record the output frequency and amplitude of the triangle wave in Table 16.7.2 and determine the deviation between the theoretical and experimental results.

7. Save the triangle and square wave display as Graph 2. Pay particular attention to the leading and trailing edges of the square wave. Are the wave shapes identical to those created with the first capacitor?

8. Return the 10n F capacitor to the circuit, replacing the 1n F unit.

9. Replace the medium speed op amps with the low speed op amps.

10. Save the triangle and square wave display as Graph 3. Pay particular attention to the leading and trailing edges of the square wave. Are the wave shapes identical to those created with the faster op amps?

16.6.1: Troubleshooting

11. Estimate and then measure the results for each individual error presented in Table 16.7.3.

16.7: Data Tables

	Theoretical	Experimental	% Deviation
f_{out}			
V_{out}			

Table 16.7.1

	Theoretical	Experimental	% Deviation
f_{out}			
V_{out}			

Table 16.7.2

Error	Quantity	Estimate	Actual
10k swapped with 22k	Square Output		
33k swapped with 22k	Triangle Output		
Input pins of Op Amp 2 swapped	Square Output		

Table 16.7.3

16.8: Questions

1. How does the oscillation frequency vary with capacitance?

2. What sets the output amplitude of the triangle and square waves?

3. By comparing Graphs 1 and 12, what sorts of non-ideal behavior occur at higher output frequencies?

4. By comparing Graphs 1 and 3, what are the advantages of using a medium speed op amp such as a 351 over a slower device such as a 741?

5. In general, what do you think the output waveforms would look like if the low speed op amps had been used with the 1n F capacitor?

CHAPTER OVERVIEW

17: The Wien Bridge Oscillator

Objective

In this exercise, a Wien bridge sine wave generator is examined. The investigation will include the effect of capacitance on output frequency and gain control of the op amp.

17.1: Theory Overview

The Wien bridge is a four element resistor-capacitor network that can be thought of as a combination of lead and lag networks. As such, it attenuates very high and very low frequencies. At its critical frequency, where the magnitude of X_c equals R, the bridge voltage produces no phase shift and exhibits a modest signal loss of 1/3. An op amp with a voltage gain of 3 may be used to overcome this loss, and as long it produces no additional phase shift, the system can produce stable oscillation at the critical frequency. A non-inverting amplifier is ideally suited to this task. The gain needs to be slightly greater than 3 to begin oscillation and should fall back to 3 to maintain oscillation. The gain variation may be achieved through the use of limiting diodes in the negative feedback network.

17.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 9.2, Op Amp Oscillators

17.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

17.4: Components

(1) Low speed op amp (741)

(1) Medium speed op amp (351, 411, 081, etc.)

(2) 1μ F

actual:___________________ ___________________

(2) 1n F

actual:___________________ ___________________

(2) 10n F

actual:___________________ ___________________

(2) 100n F

actual:___________________ ___________________

(1) 2k7 Ω

actual:___________________

(1) 5k6 Ω

actual:___________________

(3) 10k Ω

actual:___________________ ___________________ ___________________

17.5: Schematics

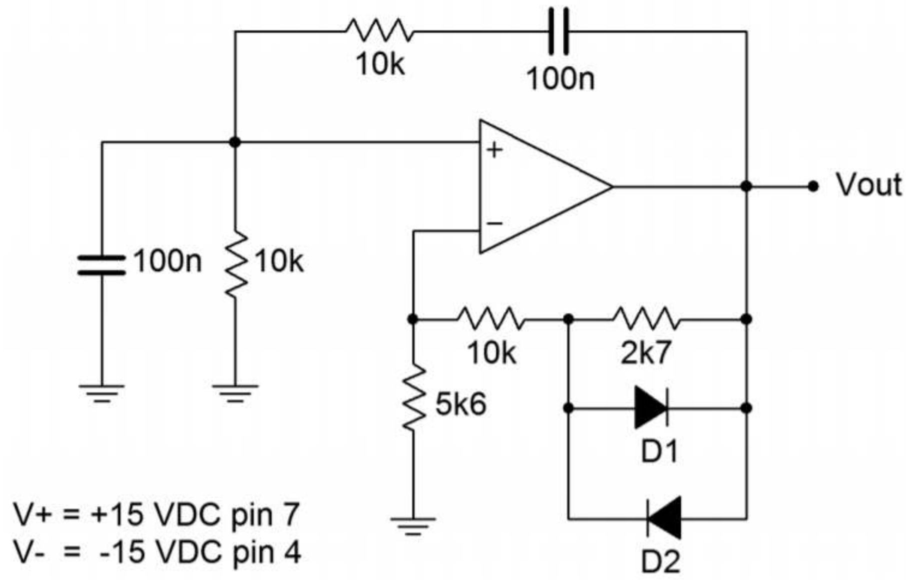

Figure 17.5.1

17.6: Procedure

1. Determine the theoretical output frequency for the circuit of Figure 17.5.1. Also, estimate the output amplitude. Record these in Table 17.7.1.

2. Construct the circuit of Figure 17.5.1 using the medium speed op amp.

3. Record the output frequency and amplitude of the sine wave in Table 17.7.1 and determine the deviation between the theoretical and experimental results.

4. Save a copy of the oscilloscope display of the output wave as Graph 1.

5. Replace the capacitors with the 10n F units. Determine the theoretical output frequency using this new value and record the result in Table 17.7.2.

6. Record the output frequency and amplitude of the wave in Table 17.7.2 and determine the deviation between the theoretical and experimental results.

7. Save a copy of the oscilloscope display of the output wave as Graph 2.

8. Replace the capacitors with the 1n F units. Determine the theoretical output frequency using this new value and record the result in Table 17.7.2.

9. Record the output frequency and amplitude of the wave in Table 17.7.2 and determine the deviation between the theoretical and experimental results.

10. Save a copy of the oscilloscope display of the output wave as Graph 3.

11. Replace the medium speed op amp with the low speed op amp and examine the output.

12. Save a copy of the oscilloscope display of the output wave as Graph 4. Swap out the capacitors with the 10n F and then the 100 nF units. Are the wave shapes identical to those created with the faster op amp?

13. In order for this circuit to oscillate, the forward gain of the op amp must compensate for the loss through the Wien bridge, in this case, a gain of 3 is required. To verify this, open the 5k6 resistor. This will drop the gain to about 1 and oscillation should cease.

17.6.1: Computer Simulation

14. One of the trickier parts of this oscillator is getting the op amp gain adjusted properly. If it is too high, the signal will be distorted. In this circuit, the initial gain is greater than 3 but as the signal grows, the two diodes turn on, partially shunting the 2k7 and reducing the effective value of R_f, and hence, the voltage gain. To demonstrate this, build the circuit in the simulator with a 741 op amp and 10n F capacitors. First perform a Transient Analysis and inspect the output wave shape. Replace the 2k7 with larger values and note the effect on the wave shape. Finally, return the resistor to 2k7, delete the two diodes and observe the new wave shape.

17.7: Data Tables

	Theoretical	Experimental	% Deviation
f_{out}			
V_{out}			

Table 17.7.1

	Theoretical	Experimental	% Deviation
f_{out}			
V_{out}			

Table 17.7.2

	Theoretical	Experimental	% Deviation
f_{out}			
V_{out}			

Table 17.7.3

17.8: Questions

1. How does the oscillation frequency vary with capacitance?

2. By comparing Graphs 1, 2, and 3, what sorts of non-ideal behavior occur at higher output frequencies?

3. By comparing Graphs 3 and 4, what are the advantages of using a medium speed op amp such as a 351 over a slower device such as a 741?

4. In general, what do you think the output waveforms would look like if the medium speed op amp had been used with a 100p F capacitor?

CHAPTER OVERVIEW

18: The Integrator

Objective

In this exercise, the concept of waveform integration will be examined. The investigation will include the effect of frequency on accurate and useful integration. Several waveshapes will be utilized.

18.1: Theory Overview

The concept of integration is usually described as “finding the area under the curve”. There are many uses for this function, including waveshaping and analog computing. An ordinary amplifier ideally changes only the amplitude of the input signal. An integrator can change the waveform of the input signal, for example, turning a square wave into a triangle wave. A practical integrator cannot be used at just any frequency. There exists a useful range of integration, outside of which the circuit does not produce the desired effect.

18.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 10.2, Integrators

18.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

18.4: Components

(1) Medium speed FET-input op amp (351, 411, 081, etc.)

(2) 1 μF

actual:___________________ ___________________

(1) 10 nF

actual:___________________

(1) 910 Ω

actual:___________________

(1) 1 kΩ

actual:___________________

(1) 10 kΩ

actual:___________________

18.5: Schematics

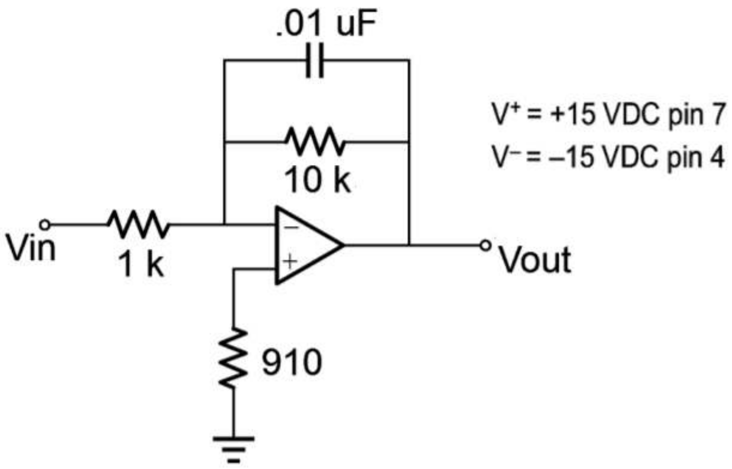

Figure 18.5.1

18.6: Procedure

1. Derive the equation for V_{out} for the circuit of Figure 18.5.1. Calculate the lowest usable (“integratable”) frequency, f_{low}. Record these items in Table 18.7.1.

2. Calculate the integrator’s output voltage for the following inputs and record them in Table 18.7.2:

- 1 volt peak sine wave at 2 times f_{low}
- 1 volt peak sine wave at 10 times f_{low}
- 1 volt peak square wave at 2 times f_{low}
- 1 volt peak square wave at 10 times f_{low}

1. Assemble the integrator circuit.

2. Save the display of the output of the integrator for each of the inputs listed in step 2, above. Call these Graphs 1 through 4, respectively. It is very important to note the phase of the output waveform with respect to the input waveform.

3. Apply a 1 volt peak sine wave one decade below f_{low}. Save the output signal as Graph 5. Does the circuit appear to be integrating?

4. Apply a 1 volt peak square wave one decade below f_{low}. Save the output signal as Graph 6. Does the circuit appear to be integrating?

18.7: Data Tables

Equation for V_{out}	
f_{low}	

Table 18.7.1

Input Signal	Output Signal
1 volt peak sine wave at 2 times f_{low}	
1 volt peak sine wave at 10 times f_{low}	
1 volt peak square wave at 2 times f_{low}	
1 volt peak square wave at 10 times f_{low}	

Table 18.7.2

18.8: Questions

1. What happens to the accuracy of integration as the input frequency is increased?

2. At very low frequencies, does the integrator behave more like a true integrator, or like an amplifier?

3. What are the advantages of using a medium speed FET-input op amp such as a 351 over a slower bipolar device such as a 741?

4. What is the purpose of the 10 kΩ resistor?

5. What is the purpose of the 910 Ω resistor?

CHAPTER OVERVIEW

19: The Differentiator

Objective

In this exercise, the concept of waveform differentiation will be examined. The investigation will include the effect of frequency on accurate and useful differentiation. Several waveshapes will be utilized.

19.1: Theory Overview

The concept of differentiation is usually described as “finding the slope of the curve.” There are many uses for this function, including waveshaping and analog computing. An ordinary amplifier ideally changes only the amplitude of the input signal. A differentiator can change the waveform of the input signal, for example, turning a triangle wave into a square wave. A practical differentiator cannot be used at just any frequency. There exists a useful range of differentiation, outside of which the circuit does not produce the desired effect.

19.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 10.3, Differentiators

19.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) DMM

model:_________________ srn:___________________

19.4: Components

(1) Medium speed FET-input op amp (351, 411, 081, etc.)

(2) 1 μF actual:___________________ ___________________

(1) 10 nF actual:___________________

(1) 1.5 nF actual:___________________

(1) 100 Ω actual:___________________

(1) 1 kΩ actual:___________________

19.5: Schematics

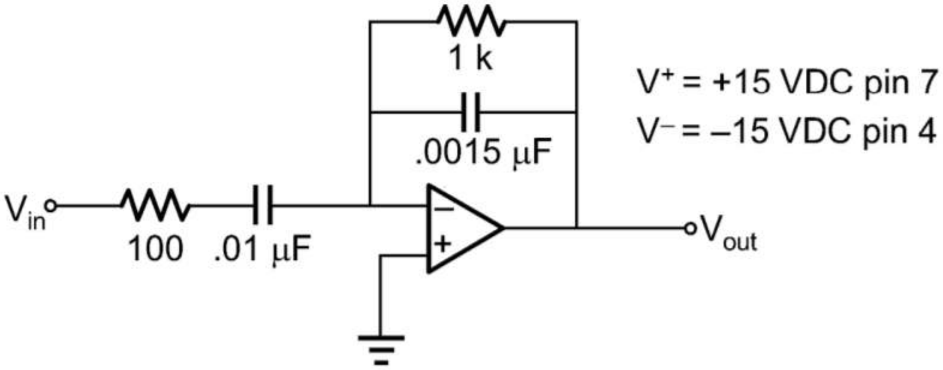

Figure 19.5.1

19.6: Procedure

1. Derive the equation for V_{out} for the circuit of Figure 19.5.1. Calculate the highest usable ("differentiable") frequency, f_{high}. Record these items in Table 19.7.1.

2. Calculate the differentiator's output voltage for the following inputs and record them in Table 19.7.2:

- 1 volt peak sine wave at one-half f_{high}
- 1 volt peak sine wave at one-tenth f_{high}
- 1 volt peak triangle wave at one-half f_{high}
- 1 volt peak triangle wave at one-tenth f_{high}

1. Assemble the differentiator circuit.

2. Save the display of the output of the differentiator for each of the inputs listed in step 2. Call these Graphs 1 through 4, respectively. It is very important to note the phase of the output waveform with respect to the input waveform.

3. Apply a 1 volt peak sine wave one decade above f_{high}. Save the output signal as Graph 5. Does the circuit appear to be differentiating?

4. Apply a 1 volt peak triangle wave one decade above f_{high}. Save the output signal as Graph 6. Does the circuit appear to be differentiating?

19.7: Data Tables

Equation for V_{out}	
f_{high}	

Table 19.7.1

Input Signal	Output Signal
1 volt peak sine wave at 1/2 f_{high}	
1 volt peak sine wave at 1/10 f_{high}	
1 volt peak triangle wave at 1/2 f_{high}	
1 volt peak triangle wave at 1/10 f_{high}	

Table 19.7.2

19.8: Questions

1. What happens to the accuracy of differentiation as the input frequency is decreased?

2. At very high frequencies, does the differentiator behave more like a true differentiator, or like an amplifier?

3. What are the advantages of using a medium speed FET-input op amp such as a 351 over a slower bipolar device such as a 741?

4. What is the purpose of the 100 Ω resistor?

5. What is the purpose of the 1.5 nF capacitor?

CHAPTER OVERVIEW

20: VCVS Filters

Objective

In this exercise, the performance of VCVS equal-component high and low pass filters will be examined. The investigation will include the realization of wide bandwidth band pass filters as well.

20.1: Theory Overview

Sallen and Key VCVS filters are very straightforward to implement, utilizing a single op amp to create second order high or low pass filters. The filters are based around a series-parallel non-inverting amplifier. In the equal component variation, the damping or alignment of the filter is set by the amplifier's pass band voltage gain. The corner frequency of the filter is set by the tuning resistors and capacitors.

20.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 11.6, Realizing Practical Filters

20.3: Equipment

(1) Oscilloscope

model:_________________ srn:___________________

(1) Function generator

model:_________________ srn:___________________

(1) Dual DC power supply

model:_________________ srn:___________________

(1) DMM capable of measuring in dB

model:_________________ srn:___________________

20.4: Components

(2) General purpose op amps (741, 351, 411, 081, etc.)

(2) 1μ F

actual:____________________ ____________________

(2) 10n F

actual:____________________ ____________________

(2) 100n F

actual:____________________ ____________________

(2) 1k5 Ω

actual:____________________ ____________________

(2) 2k2 Ω

actual:____________________ ____________________

(1) 5k6 Ω

actual:____________________

(1) 6k8 Ω

actual:____________________

(1) 10k Ω

actual:____________________

(1) 12k Ω

actual:____________________

20.5: Schematics

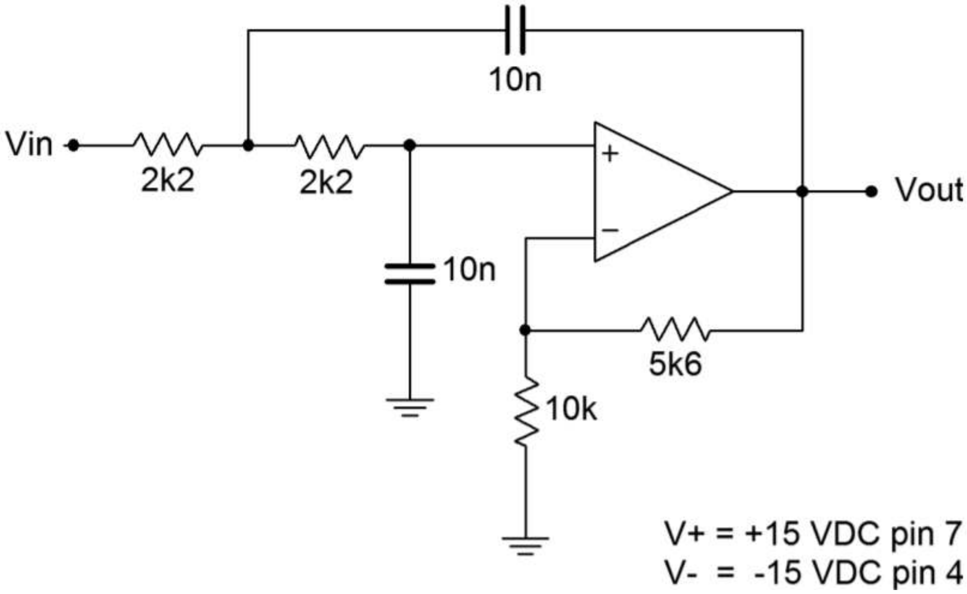

Figure 20.5.1

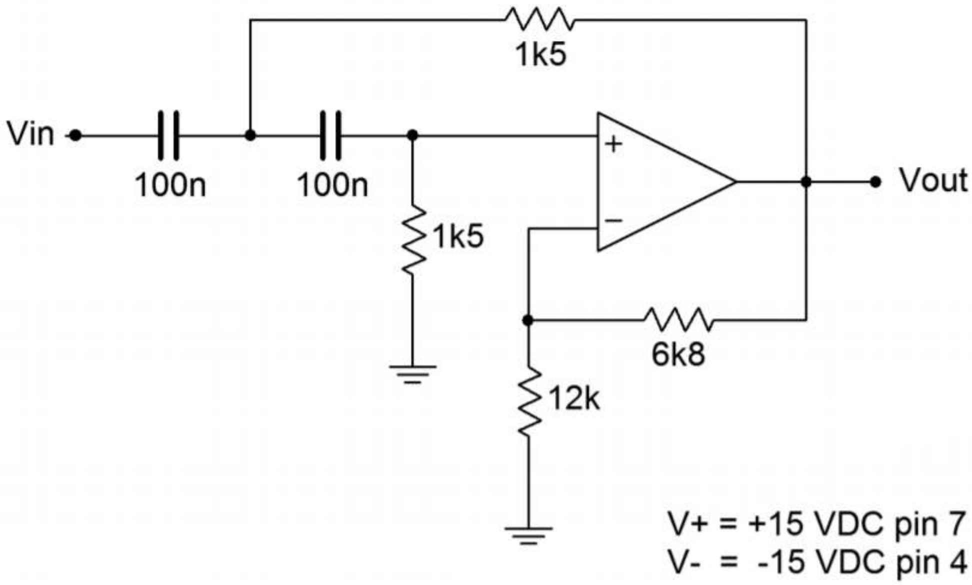

Figure 20.5.2

20.6: Procedure

20.6.1: Low Pass Filter

1. The circuit of Figure 20.5.1 is a second order low pass filter. Calculate and record the corner frequency (f_2) and mid-band voltage gain in Table 20.7.1.

2. Assemble the circuit of Figure 20.5.1.

3. To measure the mid-band voltage gain, set the generator to a 1 volt sine wave at about one decade below f_2. Measure the output of the filter and calculate the voltage gain. Record this in Table 20.7.1.

4. While monitoring the filter output with the dB meter, sweep the generator frequency about f_2 until the output has fallen 3 dB from its mid-band value. Record this frequency in Table 20.7.1.

5. In Table 20.7.2, record the dB gain of the filter at 5 frequencies between 0.1 f_2 and f_2, and at 5 frequencies between f_2 and 10 f_2. Using these data, create a semi-log plot of the frequency response of the filter. Note, it may be convenient when graphing if at least some of these frequencies are simple octaves apart, such as 5 f_2 and 10 f_2.

6. Do not disassemble the circuit.

20.6.2: High Pass Filter

7. The circuit of Figure 20.5.2 is a second order high pass filter. Calculate and record the corner frequency (f_1) and mid-band voltage gain in Table 20.7.3.

8. Assemble the circuit of Figure 20.5.2.

9. To measure the mid-band voltage gain, set the generator to a 1 volt sine wave at about one decade above f_1. Measure the output of the filter and calculate the voltage gain. Record this in Table 20.7.3.

10. While monitoring the filter output with the dB meter, sweep the generator frequency about f_1 until the output has fallen 3 dB from its mid-band value. Record this frequency in Table 20.7.3.

11. In Table 20.7.4, record the dB gain of the filter at 5 frequencies between 0.1 f_1 and f_1, and at 5 frequencies between f_1 and 10 f_1. Using these data, create a semi-log plot of the frequency response of the filter.

20.6.3: Band Pass Filter

12. Cascade the high pass and low pass filters.

13. Take several gain readings on both sides of f_1 and f_2, and record these in Table 20.7.5. Again, using these data, create a semi-log plot of the frequency response of the filter.

20.6.4: Computer Simulation

14. Build the circuit of Figure 20.5.1 in a simulator and run an AC Analysis. Be sure to run the plot from 100 Hz to approximately 100 kHz and use a decibel scale for the gain amplitude. Compare the plot to the graph generated from Table 20.7.2.

20.7: Data Tables

	Theoretical	Experimental
f_2		
A_v		

Table 20.7.1

Frequency	Gain

Table 20.7.2

	Theoretical	Experimental
f_1		
A_v		

Table 20.7.3

Frequency	Gain

Table 20.7.4

Frequency	Gain

Table 20.7.5

20.8: Questions

1. What is the approximate attenuation slope above f_2?

2. What is the approximate attenuation slope below f_1?

3. What would be the result of the cascade if the critical frequencies of the two filters were mistakenly transposed?

CHAPTER OVERVIEW

21: The Multiple Feedback Filter

Objective

In this exercise, the performance of basic band-pass filters will be examined. The investigation will include the investigation of variable Q or bandwidth.

21.1: Theory Overview

Multiple feedback filters are very straightforward to implement, utilizing a single op amp to create second order band-pass filters. The filters are based around a parallel-parallel inverting amplifier. The center frequency of the filter is set by the tuning resistors and capacitors.

21.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 11.7, Band-Pass Filter Realizations

21.3: Equipment

(1) Oscilloscope

model:________________ srn:__________________

(1) Function generator

model:________________ srn:__________________

(1) Dual DC power supply

model:________________ srn:__________________

(1) DMM capable of measuring in dB

model:________________ srn:__________________

21.4: Components

(1) Medium speed op amp (351, 411, 081, etc.)

(2) 1μ F

actual:____________________ ____________________

(2) 10n F

actual:____________________ ____________________

(2) 100n F

actual:____________________ ____________________

(1) 470 Ω

actual:____________________

(1) 1k2 Ω

actual:____________________

(1) 2k2 Ω

actual:____________________

(1) 22k Ω

actual:____________________

(1) 39k Ω

actual:____________________

(1) 47k Ω

actual:____________________

(1) 75k Ω

actual:____________________

21.5: Schematics

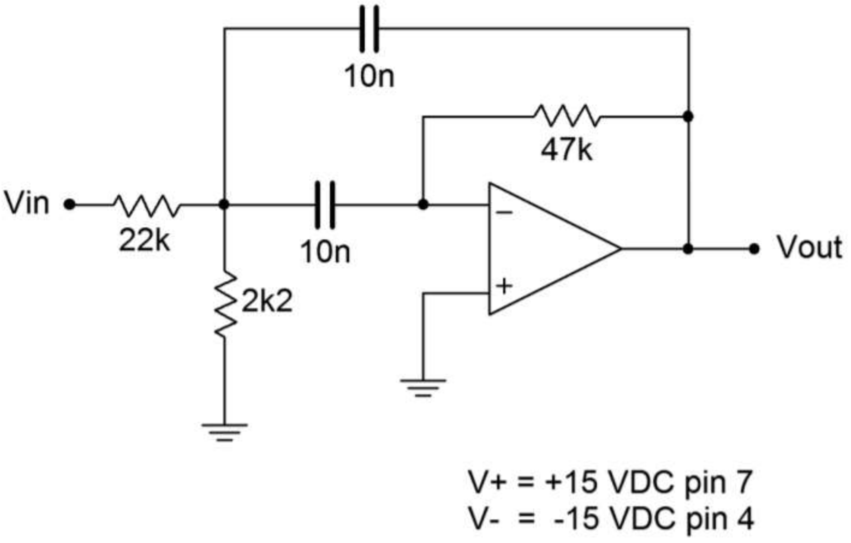

Figure 21.5.1

21.6: Procedure

1. The circuit of Figure 21.5.1 is a second order band pass filter. Calculate and record the center frequency (f_0) and mid-band voltage gain in Table 21.7.1

2. Assemble the circuit of Figure 21.5.1 using the medium speed op amp.

3. While monitoring the filter output with the dB meter, sweep the generator frequency about the expected f_0 until a peak is found. Record this frequency in Table 21.7.1. Measure the output amplitude, determine the gain and record this in Table 21.7.1 as well.

4. In Table 21.7.2, record the dB gain of the filter at 5 frequencies between 0.1 f_0 and f_0, and at 5 frequencies between f_0 and 10 f_0. Using these data, plot a graph of the filter response, and determine the bandwidth and Q of the filter.

5. Replace the capacitors with the 100n F units and repeat steps 3 and 4 using Tables 21.7.3 and 21.7.4.

6. The circuit resistors set the Q of the filter. To alter the Q of this circuit, replace the 2k2 with 1k2, the 22k with 39k, and the 47k with 75k.

7. Repeat steps 3 and 4 using Tables 21.7.5 and 21.7.6.

21.6.1: Computer Simulation

8. Build the circuit of Figure 21.5.1 in a simulator and run an AC Analysis. Be sure to run the plot from 10 Hz to approximately 100 kHz and use a decibel scale for the gain amplitude. Compare the plot to the graph generated from Table 21.7.2.

21.7: Data Tables

	Theoretical	Experimental
f_0		
A_v		

Table 21.7.1

Frequency	Gain

Table 21.7.2

	Theoretical	Experimental
f_0		
A_v		

Table 21.7.3

Frequency	Gain

Table 21.7.4

	Theoretical	Experimental
f_0		
A_v		

Table 21.7.5

Frequency	Gain

Table 21.7.6

21.8: Questions

1. For the original circuit, what is the approximate attenuation slope above f_0?

2. For the original circuit, what is the approximate attenuation slope below f_0?

3. What is the relationship between circuit capacitance and center frequency f_0?

4. How does bandwidth change as Q is altered?

5. Does the ultimate attenuation slope (i.e., at the frequency extremes) change as the Q is altered?

CHAPTER OVERVIEW

22: The State-Variable Filter

Objective

In this exercise, the performance of a state-variable filter will be examined. The investigation will include the effect of varying Q and tuning frequency.

22.1: Theory Overview

The state-variable filter, also known as the universal filter, provides several outputs, including high-pass, low-pass, and band-pass connections. The filter offers independent control over bandwidth (Q) and tuning frequency (f_c). State-variable filters are ideal for applications requiring stable, high Q response.

22.2: Reference

Fiore, Op Amps and Linear Integrated Circuits

Section 11.7, Band-Pass Filter Realizations

22.3: Equipment

(1) Oscilloscope

model:________________ srn:__________________

(1) Function generator

model:________________ srn:__________________

(1) Dual DC power supply

model:________________ srn:__________________

(1) DMM capable of measuring in dB

model:________________ srn:__________________

22.4: Components

(1) General purpose quad op amp (LM348, TL084, LF347, etc.)

(2) 1 μF

actual:____________________ ____________________

(2) 10 nF

actual:____________________ ____________________

(1) 680 Ω

actual:____________________

(2) 4.7 kΩ

actual:____________________ ____________________

(2) 6.8 kΩ

actual:____________________ ____________________

(2) 10 kΩ

actual:____________________ ____________________

(2) 15 kΩ

actual:____________________ ____________________

(1) 10 kΩ potentiometer

(1) 50 kΩ dual potentiometer

22.5: Schematics

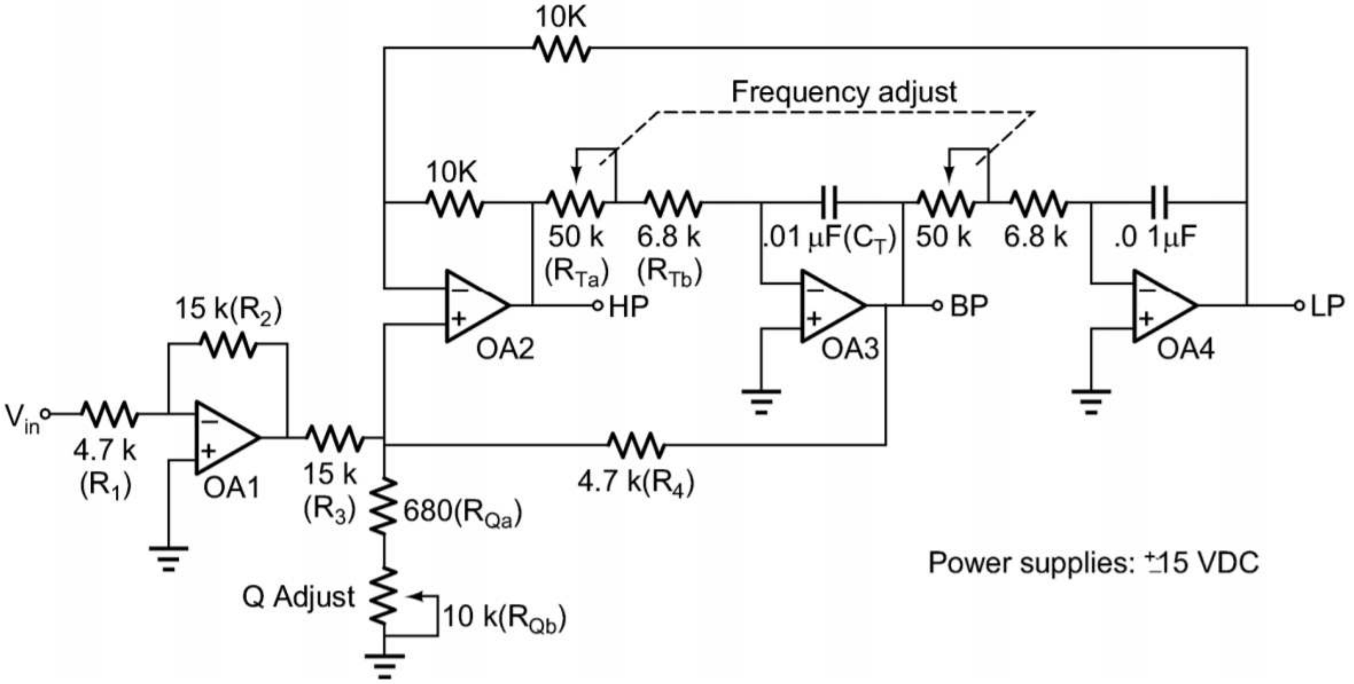

Figure 22.5.1

You will find the following formulas useful:

$f_c = 1/(2\pi R_t C_t)$

A_v (band-pass gain) = $R_2 R_4/(R_1 R_3)$

$Q = (R_x + R_4)/(2R_x)$; where $R_x = R_q || R_3$

22.6: Procedure

22.6.1: Band-pass Output

1. Assemble the circuit of Figure 22.5.1.

2. Calculate the frequency range, Q range, and band-pass gain of the filter. Record these values in Table 22.7.1. Note that R_t varies from 6.8 kΩ to 56.8 kΩ, and that R_q varies from 680 Ω to 10.68 kΩ.

3. Set Q to its highest value. This can be accomplished by adjusting the Q potentiometer for minimum resistance.

4. Apply a 0 dBV sine wave at approximately 1 kHz to the input.

5. Set the filter tuning to its highest value. This can be accomplished by adjusting R_t to minimum.

6. Sweep the input frequency until a peak output is found. Record this frequency and amplitude in Table 22.7.2.

7. Record the –3 dB, –6 dB, and –10 dB frequencies on either side of the peak, in Table 22.7.2. These amplitudes are relative to the level found at the peak.

8. Set the Q adjust to its lowest value (i.e., R_q at maximum) and repeat steps 4 through 7, using Table 22.7.3 to record your results.

9. Set the filter tuning to its minimum value (i.e., R_t at maximum) and repeat steps 4 through 8, using Tables 22.7.4 and 22.7.5 to record your results.

10. If a spectrum analyzer is available, verify your readings.

22.6.1: High- and Low-pass Outputs

11. Utilize the HP output.

12. Apply a 10 kHz sine wave to the input and adjust the amplitude for a filter output of 0 dBV.

13. By sweeping the input frequency, determine the −3 dB frequencies for R_t at both extremes. Record these values in Table 22.7.6.

14. Determine the attenuation slope by measuring the output signal amplitude using a frequency one decade below the −3 dB frequency. Record this in Table 22.7.6.

15. Utilize the LP output.

16. Apply a 100 Hz sine wave to the input and adjust the amplitude for a filter output of 0 dBV.

17. By sweeping the input frequency, determine the −3 dB frequencies for R_t at both extremes. Record these values in Table 22.7.6.

18. Determine the attenuation slope by measuring the output signal amplitude using a frequency one decade above the −3 dB frequency. Record this in Table 22.7.6.

19. If a spectrum analyzer is available, verify your readings.

22.7: Data Tables

Maximum Q	
Minimum Q	
Maximum f_c	
Minimum f_c	
Band-pass Gain	

Table $22.7.1$

Item	Frequency	Amplitude
Peak		
−3 dB, below		
−6 dB, below		
−10 dB, below		
−3 dB, above		
−6 dB, above		
−10 dB, above		

Table $22.7.2$

Item	Frequency	Amplitude
Peak		
−3 dB, below		
−6 dB, below		
−10 dB, below		
−3 dB, above		
−6 dB, above		
−10 dB, above		

Table $22.7.3$

Item	Frequency	Amplitude
Peak		
−3 dB, below		
−6 dB, below		
−10 dB, below		
−3 dB, above		
−6 dB, above		
−10 dB, above		

Table 22.7.4

Item	Frequency	Amplitude
Peak		
−3 dB, below		
−6 dB, below		
−10 dB, below		
−3 dB, above		
−6 dB, above		
−10 dB, above		

Table 22.7.5

f_{3db} for R_t at minimum	
f_{3db} for R_t at maximum	
Attenuation slope	
f_{3db} for R_t at minimum	
f_{3db} for R_t at maximum	
Attenuation slope	

Table 22.7.6

22.8: Questions

1. What is the effect as R_q is decreased?

2. What is the effect as R_t is decreased?

3. How does this filter compare to high- and low-pass VCVS filters?

4. How could this circuit be changed in order to control pass-band gain?

5. What effect would altering R_{tb} have on circuit function?

6. Why is the state-variable filter referred to as a universal filter?

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    - 1.6: Procedure - *CC BY-NC-SA 4.0*
    - 1.7: Data Tables - *Undeclared*
    - 1.8: Questions - *CC BY-NC-SA 4.0*
  - 2: The Differential Amplifier - *CC BY-NC-SA 4.0*
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    - 2.2: Reference - *Undeclared*
    - 2.3: Equipment - *CC BY-NC-SA 4.0*
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  - 3: The Op Amp Comparator - *CC BY-NC-SA 4.0*
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  - 5: The Inverting Voltage Amplifier - *CC BY-NC-SA 4.0*
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    - 7.5: Schematics - *CC BY-NC-SA 4.0*
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