10.4: JFET Biasing

There are several different ways of biasing a JFET. For many configurations, I_{DSS} and $V_{GS(off)}$ will be needed. A simple way to measure these parameters in the lab is shown in Figure 10.4.1. To measure I_{DSS} we simply ground the gate and source terminals as this forces V_{GS} to be 0 V. We insert an ammeter between V_{DD} and the drain, and then set V_{DD} to a value higher than V_P (+15 VDC generally being sufficient). The resulting ammeter reading is I_{DSS}. Obtaining $V_{GS(off)}$ is only slightly more work. Leaving the ammeter in the drain, unhook the gate from ground and instead connect it to an adjustable negative power supply. Turn the supply more negative until the ammeter reads zero (practically speaking, < 1% of I_{DSS}). At that point the voltage source will be equal to $V_{GS(off)}$.

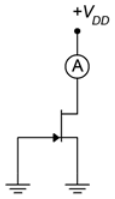

Figure 10.4.1: Measuring I_{DSS} and $V_{GS(off)}$.

10.4.1: DC Model

Before we begin examining the bias circuits themselves, we need a basic DC model of the JFET. A model sufficient for our analyses is shown in Figure 10.4.2

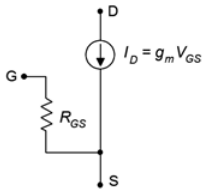

Figure 10.4.2: DC model of JFET.

The model consists of a voltage-controlled current source, I_D, that is equal to the product of the gate-source voltage, V_{GS}, and the transconductance, g_m. The resistance between the gate and source, R_{GS}, is that of the reverse-biased PN junction, in other words, ideally infinity for DC. As a consequence, in most practical circuits we can assume that gate current, I_G, is zero. Therefore, $I_D = I_S$.

10.4.2: Constant Voltage Bias

The simplest form of bias is the constant voltage bias. The prototype is shown in Figure 10.4.3 with current directions and voltage polarities shown.

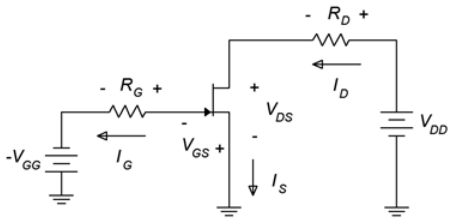

Figure 10.4.3: Constant voltage bias prototype.

This is a fairly straightforward design using only a couple of resistors and power sources. Figure 10.4.4 shows the same circuit but with the JFET model inserted, ready for analysis.

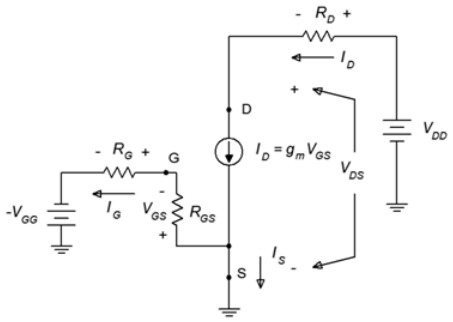

Figure 10.4.4: Constant voltage bias with model.

Ultimately, the goal here is to determine a means for finding the transistor's drain current and drain-source voltage, along with the potentials across any other components.

To begin, consider the gate-source loop. By KVL, the V_{GG} source must drop across R_G and the gate-source junction, V_{GS}.

$$V_{GG} = V_{R_G} + V_{GS}$$

$$V_{GG} = I_G R_G + V_{GS}$$

I_G is approximately zero so this simplifies to

$$V_{GS} = V_{GG}$$

Given the transconductance, g_m, we can find I_D. Alternately, I_D may be found using Equation 10.2.1 along with the device parameters I_{DSS} and $V_{GS(off)}$. For this circuit, the latter technique tends to be more practical. Once I_D is found, the voltage drop across R_D may be found, and then V_{DS} is determined from KVL.

Example 10.4.1

For the circuit of Figure 10.4.5, determine I_D and V_{DS}. Assume I_{DSS} = 10 mA and $V_{GS(off)}$ = −5 V.

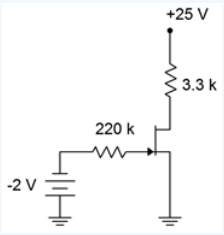

Figure 10.4.5: Schematic for Example 10.4.1.

First, because $I_G \approx 0$, the drop across R_G is ≈ 0 and $V_{GS} = V_{GG}$. Using Equation 10.2.1

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$I_D = 10mA\left(1 - \frac{-2V}{-5V}\right)^2$$

$$I_D = 3.6mA$$

Looking at the drain-source loop, KVL shows

$$V_{DD} = I_D R_D + V_{DS}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{DS} = 25V - 3.6mA \times 3.3k\Omega$$

$$V_{DS} = 13.1V$$

While the computation for the constant voltage bias is relatively simple, it does not exhibit a stable Q point. For example, if Example 10.4.1 is repeated with another JFET, this one with I_{DSS} = 12 mA and $V_{GS(off)}$ = −6 V, the results are starkly different: I_D grows to 5.33 mA and V_{DS} shrinks to 7.4 V. These are considerable changes given the relatively modest shifts in the device parameters. In this regard, the constant voltage bias is reminiscent of the simple base bias configuration used with BJTs.

To get a better understanding of the Q point stability issue, refer to Figure 10.4.6.

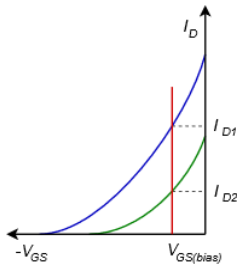

Figure 10.4.6: Variation for constant voltage bias.

Characteristic curves are plotted here for two different devices, one in green and one in blue. These represent the sort of device parameter variations we might expect to see across a product model. The fixed value of gate bias voltage is shown in red. From this graph it should be obvious that this form of bias will produce a wide variation in drain current, and thus, is not a good choice for applications that require a stable Q point. If the application does not have this requirement, constant voltage bias offers the advantage of requiring a minimum of components.

10.4.3: Self Bias

Self bias uses a small number of components and only a single power supply, yet it offers better stability than constant voltage bias. The name comes from the fact that the drain current will be used to create a voltage drop that sets up the gate-source, hence the circuit "biases itself". It is also referred to as automatic bias. The self bias prototype is shown in Figure 10.4.7.

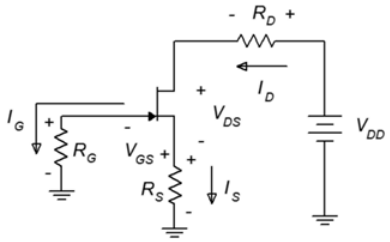

Figure 10.4.7: Self bias prototype.

Once again, we may assume that I_G is 0. As R_G is connected directly to ground, this means that $V_G \approx 0$ V. This being true, inspection of the schematic reveals that the magnitude of V_{GS} must be the same as the voltage across R_S. Because $I_D = I_S$ then

$$V_{GS} = -I_D R_S \tag{10.4.1}$$

This value of V_{GS} is what generates the drain current. The definition is self-referential. This being the case, how do we analyze the circuit? A proper derivation of the equation for drain current is not trivial. We start with the characteristic equation (Equation 10.2.1) and expand it.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$I_D = I_{DSS}\left(1 - \frac{2V_{GS}}{V_{GS(off)}} + \frac{{V_{GS}}^2}{{V_{GS(off)}}^2}\right)$$

$$I_D = I_{DSS} - \frac{2I_{DSS}V_{GS}}{V_{GS(off)}} + \frac{I_{DSS}{V_{GS}}^2}{{V_{GS(off)}}^2}$$

Substitute using Equation 10.2.2

$$g_{m0} = -\frac{2I_{DSS}}{V_{GS(off)}}$$

$$I_D = I_{DSS} + g_{m0}V_{GS} + \frac{I_{DSS}{V_{GS}}^2}{{V_{GS(off)}}^2}$$

Using Equation 10.4.1 this can be expanded to

$$I_D = I_{DSS} - g_{m0}I_D R_S + \frac{I_{DSS}{I_D}^2{R_S}^2}{{V_{GS(off)}}^2}$$

Rearranging yields

$$0 = \frac{I_{DSS}{R_S}^2}{{V_{GS(off)}}^2}{I_D}^2 - (1 + g_{m0}R_S)I_D + I_{DSS}$$

This is a quadratic equation in the form $ax^2 + bx + c$ and can be solved using the quadratic formula:

$$y = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

The positive option in the numerator may be ignored as this occurs for V_{GS} beyond $V_{GS(off)}$. The result is

$$I_D = 2I_{DSS}\left(\frac{1 + g_{m0}R_S - \sqrt{1 + 2g_{m0}R_S}}{(g_{m0}R_S)^2}\right) \tag{10.4.2}$$

Although this is an accurate analytical solution, it's certainly not the sort of equation most people want to memorize or derive as needed. As the $g_{m0}R_S$ term is repeated in this equation multiple times, it is useful to plot this equation in terms of normalized I_D versus $g_{m0}R_S$. This curve is plotted in Figure 10.4.8

To use this curve, the first step is to find $g_{m0}R_S$. The value of R_S is determined by inspection and g_{m0} may be determined by Equation 10.2.2, repeated below for convenience.

$$g_{m0} = -\frac{2I_{DSS}}{V_{GS(off)}}$$

The value of $g_{m0}R_S$ is found on the horizontal axis, traced up to the curve and then over to the normalized I_D ratio. This number is multiplied by I_{DSS} to determine the value of I_D.

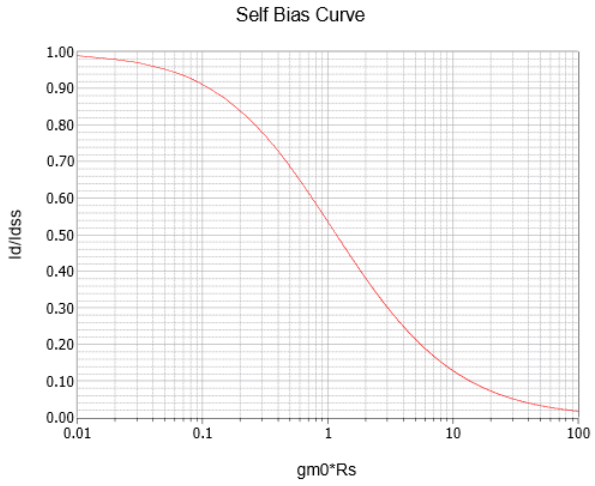

Figure 10.4.8: Self bias curve.

Example 10.4.2

Determine I_D and V_{DS} for the circuit shown in Figure 10.4.9. Assume I_{DSS} = 10 mA and $V_{GS(off)}$ = −4 V.

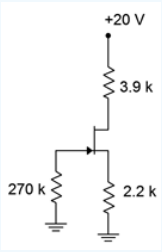

Figure 10.4.9: Schematic for Example 10.4.2

Using the graphical method, first determine $g_{m0}R_S$.

$$g_{m0} = -\frac{2I_{DSS}}{V_{GS(off)}}$$

$$g_{m0} = -\frac{2 \times 10mA}{-4V}$$

$$g_{m0} = 5mS$$

Therefore $g_{m0}R_S$ = 5 mS · 2.2 k Ω = 11. The self bias graph yields approximately 0.12 for the normalized current ratio. Therefore

$$I_D = 0.12I_{DSS}$$

$$I_D = 0.12 \times 10mA$$

$$I_D = 1.2mA$$

Using Ohm's law and KVL

$$V_D = V_{DD} - I_D R_D$$

$$V_D = 20V - 1.2mA \times 3.9k\Omega$$

$$V_D = 15.32V$$

$$V_S = I_D R_S$$

$$V_S = 1.2mA \times 2.2k\Omega$$

$$V_S = 2.64V$$

$$V_{DS} = V_D - V_S$$

$$V_{DS} = 15.32V - 2.64V$$

$$V_{DS} = 12.68V$$

An alternate technique is to make an initial guess for V_{GS}, typically one half of $V_{GS(off)}$. The value of I_D is then computed from the characteristic equation (Equation 10.2.1) and compared with the Ohm's law relation, Equation 10.4.1, rewritten as $I_D = -V_{GS}/R_S$. Chances are, the two results will not agree so adjust the V_{GS} estimate and repeat the process. If done properly, the currents should be closer. Iterate this process until you converge on the answer.

To use this technique for the preceding problem we'd start by assuming V_{GS} = −2 V (half of $V_{GS(off)}$). Using this in Equation 10.2.1 yields I_D = 2.5 mA, while using Equation 10.4.1 produces I_D = 910 μA. Obviously the initial estimate was not correct. The second estimate for V_{GS} needs to increase negatively as this will decrease the result from Equation 10.2.1 and increase the result

from Equation 10.4.1, hopefully meeting in the middle. We might try −2.5 volts. This will yield 1.4 mA from Equation 10.2.1 and 1.14 mA from Equation 10.4.1. As the gap has narrowed, the adjustment for the third estimate will be smaller, so we could try −2.6 volts. This would be relatively close to the value as computed in Example 10.4.2($V_{GS} = -V_S$).

This approximation technique also offers a clue as to how self bias gains stability over constant voltage bias. If for some reason I_D was to increase, this would create a larger voltage drop across R_S. Because this voltage is the same magnitude as V_{GS}, this means that V_{GS} grows negatively. A more negative V_{GS} reduces I_D, thus opposing the initial change in drain current. This feedback mechanism is similar in function to the BJT collector feedback bias. The stability issue is visualized in Figure 10.4.10

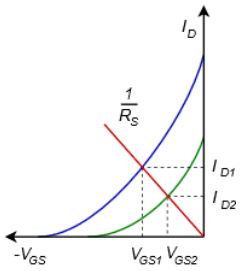

Figure 10.4.10 Variation for self bias.

Two device curves are plotted to represent parameter variation (green and blue). Equation 10.4.1 shows the relationship between I_D and V_{GS}. If we put this in the form $y = mx + b$, we find that the line goes through the origin and has a slope of $1/R_S$. This line is plotted in red. Where the line intersects the device curve yields the drain current and gate-source voltage for that particular device. Unlike constant voltage bias, self bias shifts some variation over to V_{GS}, making I_D more stable. In fact, if there is a particular design target for I_D or V_{GS}, a rearrangement of Equation 10.4.1 can be used to find the needed value of R_S along with the characteristic curve or equation.

$$R_S = -\frac{V_{GS}}{I_D}$$

For example, if a certain I_D is desired, this value could be used with Equation 10.2.1 to determine the corresponding V_{GS}. These values are then used to find the required R_S. Alternately, the normalized values could be obtained via Figure 10.2.4.

Example 10.4.3

Determine a value for R_S to set V_{GS} = −2 V for the circuit shown in Figure 10.4.11. Assume I_{DSS} = 20 mA and $V_{GS(off)}$ = −4 V.

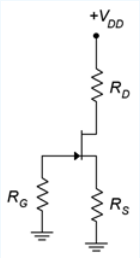

Figure 10.4.11: Schematic for Example 10.4.3

We can determine the drain current using Equation 10.2.1.

$$I_D = I_DSS\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$I_D = 20mA\left(1 - \frac{-2V}{-4V}\right)^2$$

$$I_D = 5mA$$

$$R_S = -\frac{V_{GS}}{I_D}$$

$$R_S = -\frac{-2V}{5mA}$$

$$R_S = 400\Omega$$

In sum, self bias is a minimal parts count circuit that offers modest stability. The stability can be improved with the addition of other components, as we shall see with the next bias configuration.

10.4.4: Combination Bias

The combination bias configuration (AKA source bias) is based on self bias but adds a negative power supply connected to R_S, hence its name. This will enhance the stability of I_D, V_{DS} and g_m. The combination bias prototype is shown in Figure 10.4.12

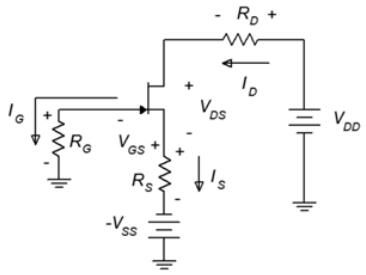

Figure 10.4.12 Combination bias prototype.

The analysis is similar to that of self bias but with one major twist: the source power supply increases the voltage drop across R_S. This stabilizes the voltage (and hence, the current) because it is no longer equal to $-V_{GS}$, but rather

$$V_{R_S} = I_D R_S = \mid V_{GS} \mid + \mid V_{SS} \mid \tag{10.4.3}$$

If $V_{SS} \gg V_{GS}$, then we can approximate I_D as V_{SS}/R_S. As with self bias, an analytical solution for I_D is possible. In order to do so, we would begin with the characteristic equation and Equation 10.4.3. The derivation is left as an exercise.

$$I_D = 2I_{DSS}\left(\frac{1+g_{m0}R_S(1+k)-\sqrt{1+2g_{m0}R_S(1+k)}}{(g_{m0}R_S)^2}\right) \tag{10.4.4}$$

The formula is very similar to the self bias formula but with the addition of a factor, k. k is a "swamping factor" and is defined as the ratio of V_{SS} to $V_{GS(off)}$. If $k = 0$, there is no source power supply and the formula reverts back to the simpler self bias formula. On the other hand, if k is very large, $I_D \approx V_{SS}/R_S$.

As was the case with self bias, we can plot Equation 10.4.4 using the $g_{m0}R_S$ factor. A series of three plots for k = 2, 3 and 4 are rendered in Figured 10.4.13[1]

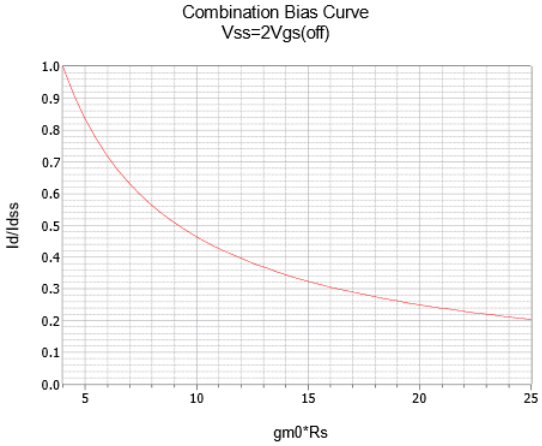

Figure 10.4.13a Combination bias curve, $k = 2$.

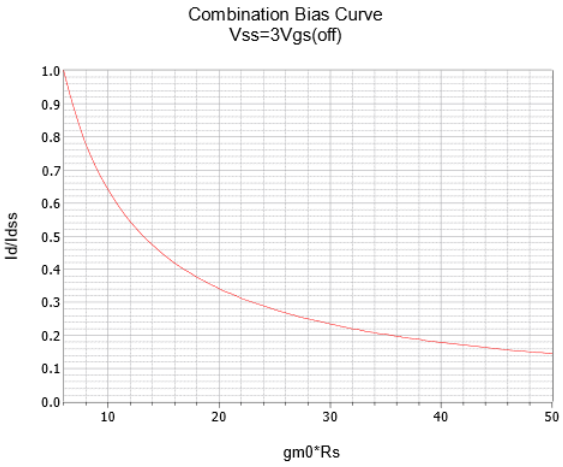

Figure 10.4.13b Combination bias curve, $k = 3$.

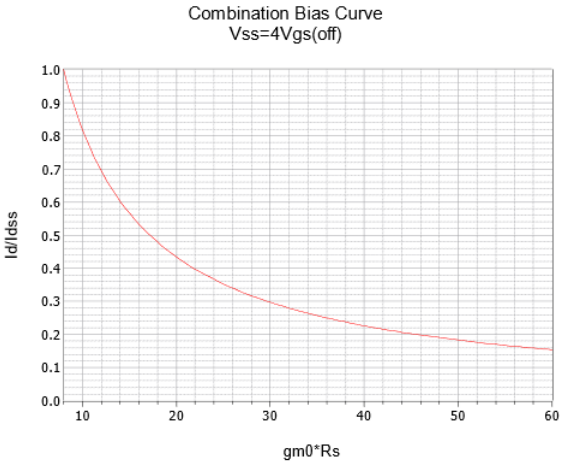

Figure 10.4.13c Combination bias curve, $k = 4$.

Example 10.4.4

Determine I_D and V_{DS} for the circuit shown in Figure 10.4.14 Assume I_{DSS} = 12 mA and $V_{GS(off)}$ = −4 V.

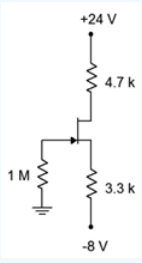

Figure 10.4.14 Schematic for Example 10.4.4

Using the graphical method, first determine $g_{m0}R_S$.

$$g_{m0} = -\frac{2I_{DSS}}{V_{GS(off)}}$$

$$g_{m0} = -\frac{2 \times 12mA}{-4V}$$

$$g_{m0} = 6mS$$

Therefore $g_{m0}R_S$ = 6 mS · 3.3 k Ω = 19.8. The swamping ratio, k, is $V_{SS}/V_{GS(off)} = -8/-4 = 2$. This requires the graph in Figure $10.4.13a$ This graph yields approximately 0.25 for the normalized current ratio. Therefore

$$I_D = 0.25 I_{DSS}$$

$$I_D = 0.25 \times 12mA$$

$$I_D = 3mA$$

Using Ohm's law and KVL

$$V_D = V_{DD} - I_D R_D$$

$$V_D = 24V - 3mA \times 4.7k\Omega$$

$$V_D = 9.9V$$

$$V_S = V_{SS} + I_D R_S$$

$$V_S = -8V + 3mA \times 3.3k\Omega$$

$$V_S = 1.9V$$

$$V_{DS} = V_D - V_S$$

$$V_{DS} = 9.9V - 1.9V$$

$$V_{DS} = 8V$$

As a crosscheck, using Equation 10.4.4 yields 3.028 mA for I_D. The deviation is no doubt due to inaccuracy in reading the graph. In any case, using this value of drain current we find V_S to be 1.992 volts, a little higher than calculated above. This indicates that V_{GS} is −1.992 volts (because $V_G \approx 0$ V). If we plug this value of V_{GS} into Equation 10.2.1, $I_D = 3.024$ mA; an excellent match with the deviation being due to accumulated rounding errors.

In order to show the increased Q point stability of the combination bias, we'll repeat the preceding problem using a JFET with a significantly lower I_{DSS}.

Example 10.4.5

Determine I_D for the circuit shown in Figure $10.4.14$ Assume I_{DSS} = 8 mA and $V_{GS(off)}$ = −4 V.

For this version we'll use Equation 10.4.4. First determine $g_{m0}R_S$.

$$g_{m0} = -\frac{2I_{DSS}}{V_{GS(off)}}$$

$$g_{m0} = -\frac{2 \times 8mA}{-4V}$$

$$g_{m0} = 4mS$$

Therefore $g_{m0}R_S$ = 4 mS · 3.3 k Ω $= 13.2$. The swamping ratio, k, is $V_{SS}/V_{GS(off)} = -8/-4 = 2$.

$$I_D = 2I_{DSS}\left(\frac{1 + g_{m0}R_S(1+k) - \sqrt{1 + 2g_{m0}R_S(1+k)}}{(g_{m0}R_S)^2}\right)$$

$$I_D = 2 \times 8mA\left(\frac{1 + 13.2(1+2) - \sqrt{1 + 2 \times 13.2(1+2)}}{(13.2)^2}\right)$$

$$I_D = 2.906mA$$

For the graphical method, a reasonable estimate for the normalized I_D would be around 0.36, yielding a drain current of 2.88 mA. Stability is apparent because the drain current has dropped only a few percent in spite of the fact that I_{DSS} decreased by 33%.

The graph of Figure 10.4.15 illustrates nicely the increased stability of the Q point. Once again, we plot two representative device curves in green and blue. As was the case with self bias, a plot line can be drawn, the slope of which is equal to the reciprocal of R_S. This plot line does not go though the origin, though. Instead, the x axis intercept is the voltage $|V_{SS}|$. Thus, the red plot line is shifted along the V_{GS} axis.

As can be seen in the graph, the variation in I_D is reduced (although at the expense of variation in V_{GS}). For large values of V_{SS} with correspondingly large values of R_S, the bias plot line becomes nearly horizontal, indicating a very stable Q point. With two variables in play, this bias proves to be very flexible. It can also be realized by using a positive voltage divider at the gate and removing V_{SS} (returning R_S to ground).

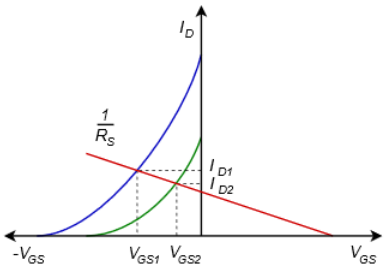

Figure 10.4.15: Variation for combination bias.

10.4.5: Constant Current Bias

The most stable bias for JFETs relies, oddly enough, on a current source made with a BJT. It is called constant current bias, yet another imaginative tag. Interestingly, although this will keep the Q point very stable, a fixed I_D does not guarantee the most stable value of voltage gain. In fact, it might be easier to achieve that goal using combination bias. The prototype constant current bias circuit is shown in Figure 10.4.16. An NPN BJT is used for an N-channel JFET and a PNP would be used with a P-channel JFET, typically driven from above (i.e., circuit flipped top to bottom).

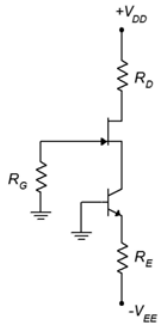

Figure 10.4.16: Constant current bias prototype.

Ignoring the JFET for a moment, the BJT is configured as in two-supply emitter bias. In this case the base is tied directly to ground, leaving the emitter at about −0.7 VDC. The remainder of the V_{EE} supply drops across R_E, establishing the emitter current. As the collector is connected directly to the JFET's source terminal, this means that $I_S \approx I_E$. The source current winds up being just as stable as the emitter current, which we have already seen is very stable. The only requirement is that I_E should not be programmed to be larger than I_{DSS}. This being true, I_D will set up a corresponding V_{GS}. This also establishes V_S because $V_G \approx 0$ V. Therefore, the source terminal will be a small positive voltage and this is precisely what the BJT needs in order to guarantee that its collector-base junction is reverse-biased.

Computation of circuit currents and voltages is straightforward and does not involve the use of graphical aides. The first step is to examine the BJT's emitter loop and determine I_E. Once this is found, I_S and I_D are known, and all remaining component potentials may be found using Ohm's law and KVL.

This technique does not involve the calculation of V_{GS}. In fact, because I_D is very stable, V_{GS} will show the widest variation of all biasing circuits when the JFET is changed. If V_{GS} is needed, it can be determined via a little algebraic manipulation on Equation 10.2.1.

Example 10.4.6

Detemine I_D, V_{DS} and V_{GS} in the circuit of Figure 10.4.17. I_{DSS} = 15 mA and $V_{GS(off)}$ = −3 V.

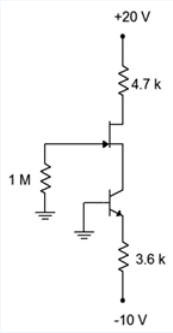

Figure 10.4.17: Schematic for Example 10.4.6

We begin by finding I_E.

$$I_E = \frac{|V_{EE}| - 0.7V}{R_E}$$

$$I_E = \frac{10V - 0.7V}{3.6k\Omega}$$

$$I_E = 2.58mA$$

I_E is the same as I_S and I_D, therefore

$$V_D = V_{DD} - I_D R_D$$

$$V_D = 20V - 2.58mA \times 4.7k\Omega$$

$$V_D = 7.87V$$

To find V_S we note that $V_S = -V_{GS}$ and rearrange Equation 10.2.1.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$V_{GS} = V_{GS(off)}\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$V_{GS} = -3V\left(1 - \sqrt{\frac{2.58mA}{15mA}}\right)$$

$$V_{GS} = -1.24V$$

Therefore $V_S = 1.24$ V and

$$V_{DS} = V_D - V_S$$

$$V_{DS} = 7.87V - 1.24V$$

$$V_{DS} = 6.63V$$

We turn next to a computer simulation of a similar circuit to validate our methodology.

Computer Simulation

A constant current bias circuit is entered into a simulator as shown in Figure 10.4.18

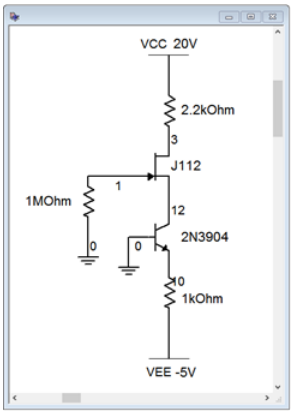

Figure 10.4.18 Constant current bias circuit in simulator.

A cursory estimate shows that I_E and I_D should be around 4.3 mA. Also, V_D should be approximately 20 V − 4.3 mA · 2.2 kΩ, or about 10.54 volts. The results of a DC operating point analysis are shown in Figure 10.4.19

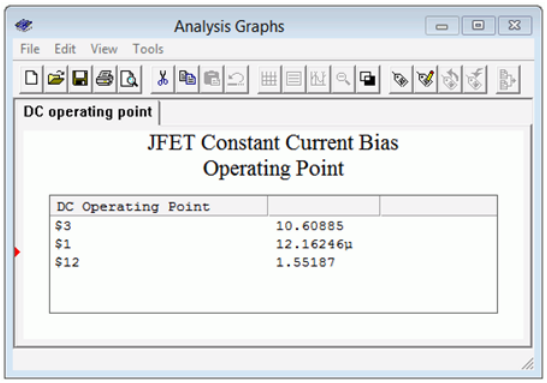

Figure 10.4.19 Constant current bias DC operating point simulation results.

The drain voltage (node 3) is just over 10.6 volts, agreeing with our estimate. Also, note the minuscule gate voltage (node 1) of 12 μV which verifies our continuing assumption in these circuits that $V_G \approx 0$ VDC. Finally, we see a modest potential of about 1.5 volts at the source terminal (node 12). This shows the proper reverse-biasing of both the gate-source and collector-base junctions.

Finally, we can examine the Q point variation using Figure 10.4.20 Here, the plot line is perfectly horizontal and all device variation is manifest in V_{GS}.

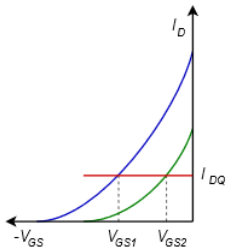

Figure 10.4.20 Variation for constant current bias.

References

[1]We could add a third axis for k and plot a surface, and while it might be pretty, a 3D plot like this rendered onto a 2D surface, such as a page in a textbook, is of marginal utility.